I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2001-205188 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date of Application: July 5, 2001

Application Number: Japanese Patent Application No. 2001-205188

Applicant(s) FUJITSU LIMITED

September 27, 2001

Commissioner,
Patent Office Kouzo Oikawa (Seal)

Certificate No.2001-3088874

日　本　国　特　許　庁
JAPAN　PATENT　OFFICE

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出願年月日
Date of Application:　２００１年　７月　５日

出願番号
Application Number:　特願２００１－２０５１８８

出願人
Applicant(s):　富士通株式会社

２００１年　９月２７日

特許庁長官
Commissioner,
Japan Patent Office　及川耕造

出証番号　出証特２００１－３０８８８７４

(Document Name)	Application For Patent
(Reference Number)	0140691
(Date of Submission)	July 5, 2001
(Destination)	Commissioner of Patent Office Mr. kouzo Oikawa
(IPC)	H01L 27/08 H01L 21/76 H01L 21/94
(Title of the Invention)	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF PRODUCING THE SAME
(Number of Claims)	10
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(Indication of Official Fees)	
(Prepayment Ledger Number)	002989
(Amount Paid)	¥21,000
(Lists of Submitted Documents)	
(Document Name)	Specification 1
(Document Name)	Drawing 1
(Document Name)	Abstract 1
(Number of General Power of Attorney)	9704678
(Proof Requested or Not)	Requested

[Name of the Document] Specification

[Title of the Invention] SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF PRODUCIING THE SAME

[Claims]

[Claim 1]

A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of the substrate; and

a semiconductor device formed in a device region of the substrate,

the nonvolatile memory device having a multilayer gate electrode structure including a tunnel insulating film covering the surface of the substrate in the memory cell region, a floating gate electrode formed on the tunnel insulating film, an insulating film formed on the floating gate electrode, and a control gate electrode formed on the insulating film,

the semiconductor device including a gate insulating film covering the surface of the substrate in the device region and a gate electrode formed on the gate insulating film,

the floating gate electrode having sidewall surfaces covered with a protection insulating film formed of a thermal oxide film, wherein

a bird's beak structure, which is formed of a thermal oxide film and penetrates into the floating gate electrode along an interface from the sidewall surfaces of the floating gate electrode, is formed at the interface of the tunnel insulating film and the floating gate electrode, and

gate insulating film is interposed between the surface of the substrate and the undersurface of the gate electrode to have a substantially uniform thickness.

[Claim 2]

A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of the substrate; and

a semiconductor device formed in a device region of the substrate,

the nonvolatile memory device including

a first active region formed in the memory cell region and covered with a tunnel insulating film, a second active region formed next to the first active region and covered with an insulating film in the memory cell region, a control gate formed of an embedded diffusion region formed in the second active region, a first gate electrode extending on the tunnel insulating film in the first active region and forming a bridge between the first and second active regions in the memory cell region to be capacitive-coupled via the insulating film and the embedded diffusion region in the second active region, and a pair of diffusion regions formed on each of sides of the first gate electrode in the first active region,

the semiconductor device being formed of a gate insulating film covering the surface of the substrate in the device region and a second gate electrode formed on the gate insulating film,

the first gate electrode having side wall surfaces thereof covered with a protection insulating film formed of a thermal oxide film, wherein

a bird's beak structure, which is formed of a thermal oxide film and penetrates into the first gate electrode along an interface from the sidewall surfaces of the first gate electrode, is formed at the interface of the tunnel insulating film and the first gate electrode, and the gate oxide film is interposed between the surface of the substrate and the undersurface of the second gate electrode to have a substantially uniform thickness.

[Claim 3]

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film covering the first silicon film in the memory cell region, a first gate insulating film covering the first device region, and a second gate insulating film covering the second device region and thicker than the first gate insulating film;

depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region, the first gate insulating film in the first device region, and the second gate insulating film in the second device region;

forming a multilayer gate electrode structure in

the memory cell region by selectively patterning the second silicon film, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the first and second device regions;

forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the first and second device regions;

forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks;

forming first and second gate electrodes in the first and second device regions by patterning the second silicon film; and

forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[Claim 4]

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first gate insulating film covering the first device region, and a second gate insulating film covering the

second device region and thicker than the first gate insulating film;

depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region, the first gate insulating film in the first device region, and the second gate insulating film in the second device region;

forming a third gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the first and second device regions;

forming a protection oxide film so that the protection oxide film covers the third gate electrode in the memory cell region and the surface of the silicon film in the first and second device regions;

forming diffusion regions in both sides of the third gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the third gate electrode and the silicon film being employed as masks;

forming first and second gate electrodes in the first and second device regions by patterning the silicon film; and

forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[Claim 5]

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate where the memory cell region and the logic device region are

defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film covering the first silicon film in the memory cell region, and a gate insulating film covering the logic device region;

depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region and the gate insulating film in the logic device region;

forming a multilayer gate electrode structure in the memory cell region by selectively patterning the second silicon film to be a control gate electrode, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the logic device region;

forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the logic device region;

forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks;

forming gate electrodes in the logic device region by patterning the second silicon film; and

forming diffusion regions in the logic device region by performing ion implantation with the gate electrodes being employed as masks.

[Claim 6]

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate where the memory cell region and the logic device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate and a gate insulating film covering the logic device region;

depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region and the gate insulating film in the logic device region;

forming a first gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the logic device region;

forming a protection oxide film so that the protection oxide film covers the first gate electrode in the memory cell region and the surface of the silicon film in the logic device region;

forming diffusion regions in both sides of the first gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the first gate electrode and the silicon film being employed as masks;

forming a second gate electrode in the logic device region by patterning the silicon film; and

forming diffusion regions in the logic device region by performing ion implantation with the second gate electrode being employed as a mask.

[Claim 7]

The semiconductor integrated circuit device as claimed in claim 1, wherein each of the gate electrode and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

[Claim 8]

The semiconductor integrated circuit device as claimed in claim 2, wherein the second gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

[Claim 9]

The semiconductor integrated circuit device as claimed in claim 1, 2, 7, or 8, wherein the thermal oxide film forming the protection insulating film connects to the bird's beak structure.

[Claim 10]

The method as claimed in any one of claims 3 through 6, wherein each of the gate electrode, the first gate electrode, the second gate electrode, and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention generally relates to semiconductor integrated circuit devices and methods of producing the same, and more particularly to a semiconductor device including a nonvolatile semiconductor storage device

and using a plurality of supply voltages, and a method of producing such a semiconductor integrated circuit device.

[0002]

A flash memory device is a nonvolatile semiconductor storage device that stores information in the form of electric charges in floating gate electrodes. The flash memory device" which has a simple device configuration, is suitable for forming a large-scale integrated circuit device.

[0003]

In the flash memory device, information is written or erased by injecting hot carriers into and extracting hot carriers by the Fowler-Nordheim-type tunnel effect from the floating gate electrodes through a tunnel insulating film. Since a high voltage is required to generate such hot carriers, the flash memory device has a voltage rise control circuit that raises a supply voltage provided in its peripheral circuits cooperating with memory cells. Therefore, transistors used in such peripheral circuits have to operate at a high voltage.

[0004]

On the other hand, it has been practiced of late to form such a flash memory device and a high-speed logic circuit on a common semiconductor substrate as a semiconductor integrated circuit device. In such a high-speed logic circuit, a transistor employed therein is required to operate at a low voltage. Therefore, such a semiconductor integrated circuit device is required to use a plurality of supply voltages.

[0005]

[Prior Art]

FIGS. 1(A) through 9(Q) are diagrams showing a production process of the conventional semiconductor integrated circuit device including such a flash memory and using a plurality of supply voltages.

[0006]

In FIG. 1(A), a flash memory cell region A, a low-voltage operation transistor region B, and a high-voltage operation transistor region C are formed in partitions on a silicon (Si) substrate 11 on which a field oxide film or an isolation structure (not shown in the drawing) such as a shallow trench isolation (STI) structure is formed. In the step of FIG. 1(A), a tunnel oxide film 12A of a thickness of 8 to 10 nm is formed on the above-described regions A through C by performing thermal oxidation on the surface of the Si substrate 11 at temperatures ranging from 800 to 1100 °C. In the step of FIG. 1(B), an amorphous silicon film 13 doped with phosphorous (P) and having a thickness of 80 to 120 nm and an insulating film 14 having a so-called oxide-nitride-oxide (ONO) structure are successively deposited on the tunnel oxide film 12A. The ONO insulating film 14 is formed of a silicon dioxide (SiO2) film 14c of a thickness of 5 to 10 nm deposited by chemical vapor deposition (CVD) on the amorphous silicon film 13, a silicon nitride (SiN) film 14b of a thickness of 5 to 10 nm deposited by CVD on the SiO2 film 14c, and a thermal oxide film 14a of a thickness of 3 to 10 nm formed on the surface of the SiN film 14b. The ONO insulating film 14 has a good leakage-current characteristic.

[0007]

Next, in the step of FIG. 2(C), a resist pattern

15A is formed on the flash memory cell region A, and the ONO insulating film 14, the amorphous silicon film 13, and the tunnel oxide film 12A are removed from the low-voltage operation transistor region B and the high-voltage operation transistor region C on the Si substrate 11 by using the resist pattern 15A as a mask so that the surface of the Si substrate 11 is exposed in the regions B and C. In removing the tunnel oxide film 12A, wet etching using hydrofluoric acid (HF) is performed so that the surface of the Si substrate 11 is exposed to the HF in the regions B and C.

[0008]

In the step of FIG. 2(D), the resist pattern 15A is removed, and a thermal oxide film 12C of a thickness of 10 to 50 nm is formed in the regions B and C to cover the Si substrate 11 by performing thermal oxidation at temperatures ranging from 800 to 1100 °C. The thermal oxide film 12C may be replaced by a thermal nitride oxide film.

[0009]

In the step of FIG. 3(E), another resist pattern 15B is formed in the flash memory cell region A to cover the ONO insulating film 14 and in the high-voltage transistor region C to cover the thermal oxide film 12C, and the thermal oxide film 12C is removed from the low-voltage operation transistor region B by HF processing by using the resist pattern 15B as a mask so that the surface of the Si substrate 11 is exposed in the region B. By the step of FIG. 3(E), the surface of the Si substrate 11 is subjected to the second HF processing in the region B.

[0010]

In the step of FIG. 3(F), the resist pattern 15B

is removed, and a thermal oxide film 12B of a thickness of 3 to 10 nm is formed on the exposed Si substrate 11 in the region B by performing thermal oxidation at temperatures ranging from 800 to 1100 °C. The thermal oxide film 12B may be replaced by a thermal nitride oxide film. Further, in the step of FIG. 3(F), as a result of the thermal oxidation for forming the thermal oxide film 12B, the thickness of the thermal oxide film 12C formed in the high-voltage operation transistor region C increases.

[0011]

Next, in the step of FIG. 4(G), an amorphous silicon film 16 doped with p and having a thickness of 100 to 250 nm is deposited on the structure of FIG. 3(F) by plasma CVD. The amorphous silicon film 16 may be replaced by a polysilicon film. Further, the amorphous silicon film 16 may be doped with p in a later step. In the step of FIG. 4(H), by using the resist pattern 17A as a mask, patterning is performed successively on the amorphous silicon film 16, the ONO insulating film 14, and the amorphous silicon film 13, so that a multilayer gate electrode structure 16F of the flash memory whose structure is formed of an amorphous silicon pattern 13A, an ONO pattern 14A, and an amorphous silicon pattern 16A and which includes the amorphous silicon pattern 13A as a floating gate electrode, is formed in the region A. In the step of FIG. 4G, it is possible to form a silicide film of, for instance, tungsten silicide (WSi) or cobalt silicide (CoSi) on the amorphous silicon film 16 as required. Further, it is also possible to form a non-doped polysilicon film and then form an n-type gate electrode of p or arsenic (As) or a p-type gate electrode of boron (B) or difluoroboron (BF2) in a later step of ion implantation.

[0012]

Next, in the step of FIG. 5(I), the resist pattern 17A is removed, and a new resist pattern 17B is formed to cover the flash memory cell region A. By using the resist pattern 17B as a mask, patterning is performed on the amorphous silicon film 16 in the low-voltage operation transistor region B and the high-voltage operation transistor region C, so that a gate electrode 16B of a low-voltage operation transistor and a gate electrode 16C of a high-voltage operation transistor are formed in the regions B and C, respectively.

[0013]

Next, in the step of FIG. 5(J), the resist pattern 17B is removed, and a protection oxide film 18 is formed, by performing thermal oxidation at temperatures ranging from 800 to 900 °C, to cover each of the multilayer gate electrode structure 16F in the flash memory cell region A, the gate electrode 16B in the low-voltage operation transistor region B, and the gate electrode 16C in the high-voltage operation transistor region C.

[0014]

Next, in the step of FIG. 6(K), a resist pattern 19A is formed on the structure of FIG. 5(J) so as to cover the low-voltage operation transistor region B, the high-voltage operation transistor region C, and a part of the flash memory cell region A. By using the resist pattern 19A and the multilayer gate electrode structure 16F as masks, ion implantation of p+ is performed typically with a dose of 1×10^{14} to 3×10^{14} cm^{-2} at accelerating voltages ranging from 30 to 80 keV so that an n-type diffusion region 11a is formed next to the multilayer gate electrode structure 16F in the

Si substrate 11. p^+ may be replaced by As^+.

[0015]

In the step of FIG. 6(K), by using the resist pattern 19A as a mask, ion implantation of As^+ is performed typically with a dose of 1×10^{15} to 6×10^{15} cm^{-2} at accelerating voltages ranging from 30 to 50 keV so that another n-type diffusion region 11b is formed inside the n-type diffusion region 11a. In the step of FIG. 6(K), no ion implantation is performed in the low-voltage operation transistor region B and the high-voltage operation transistor region C since the regions B and C are covered with the resist pattern 19A.

[0016]

Next, in the step of FIG. 6(L), the resist pattern 19A is removed, and a new resist pattern 19B is formed to cover the regions B and C and leave the region A exposed. Further, in the step of FIG. 6(L), by using the resist pattern 19B as a mask, ion implantation of As^+ is performed with a dose of 5×10^{14} to 5×10^{15} cm^{-2} at accelerating voltages ranging from 30 to 50 keV. As^+ may be replaced by p^+. As a result, an impurity concentration is increased in the n-type diffusion region 11b and at the same time, a yet another n-type diffusion region 11c is formed in the flash memory cell region A by using the multilayer gate electrode structure 16F as a self-alignment mask. At this point, the step of FIG. 6(K) may be deleted.

[0017]

Next, in the step of FIG. 7(M), the resist pattern 19B is removed, and a resist pattern 19C is formed on the Si substrate 11 so as to leave only the low-voltage operation transistor region B exposed. Further, in the step of FIG.

7(M), ion implantation of a p-type or n-type impurity is performed by using the resist pattern 19C as a mask so that a pair of lightly doped drain (LDD) diffusion regions 11d are formed on both sides of the gate electrode 16B in the Si substrate 11 in the region B with the gate electrode 16B serving as a self-alignment mask.

[0018]

Next, in the step of FIG. 7(N), the resist pattern 19C is removed, and a resist pattern 190 is formed on the Si substrate 11 so as to leave only the high-voltage operation transistor region C exposed. Further, in the step of FIG. 7(N), ion implantation of a p-type or n-type impurity element is performed by using the resist pattern 19D as a mask so that a pair of LDD diffusion regions 11e are formed on both sides of the gate electrode 16C in the Si substrate 11 in the region C. The diffusion regions 11d and 11e may be formed in the same step.

[0019]

Further, in the step of FIG. 8(O), sidewall insulating films 16s are formed on both sides of each of the multilayer gate electrode structure 16F, the gate electrode 16B, and the gate electrode 16C by depositing and performing etchback on a CVD oxide film. In the step of FIG. 8(P), a resist pattern 19E covering the flash memory cell region A is formed to expose the low-voltage operation transistor region B and the high-voltage operation transistor region C. Further, by performing ion implantation of a p-type or n-type impurity element with the resist pattern 19E and the gate electrodes B and C serving as a mask, p-type or n-type diffusion regions 11f are formed on both sides of the gate electrode 16B in the Si substrate 11 in the region B.

Similarly, p-type or n-type diffusion regions 11g are formed on both sides of the gate electrode 16C in the Si substrate 11 in the region C. A low-resistance silicide film of, for instance, WSi or CoSi may be formed as required on the surface of each of the diffusion regions 11f and 11g by silicide processing.

[0020]

In the step of FIG. 9(Q), an interlayer insulating film 20 is formed on the Si substrate 11 so as to continuously cover the regions A through C. Further, in the region A, contact holes are formed in the interlayer insulating film 20 so that the diffusion regions 11b and 11c are exposed, and W plugs 20A are formed in the contact holes. Likewise, in the region B, contact holes are formed in the interlayer insulating film 20 so that the diffusion regions 12f are exposed, and W plugs 20B are formed in the contact holes. In the region C, contact holes are formed in the inter layer insulating film 20 so that the diffusion regions 12g are exposed, and W plugs 20C are formed in the contact holes.

[0021]

[Problems to be Solved by the Invention]

In the production process of the semiconductor integrated circuit device including the flash memory device having the multilayer gate electrode structure 16F, in the step of FIG. 5(J), the protection oxide film 18 of a thickness of 5 to 10 nm is formed on the sidewall faces of the multilayer gate electrode structure 16F by thermal oxidation performed at temperatures ranging from 800 to 900 °C. As a result of the thermal oxidation, the protection oxide film 18 is formed not only on the multilayer gate electrode structure 16F but also on the sidewall faces of each of the gate electrode 16B

formed in the low-voltage operation transistor region B and the gate electrode 16C formed in the high-voltage operation transistor region C as shown in FIGS. 10(A) and 10(B).

[0022]

At this point, the protection oxide film 18 forms bird's beaks that penetrate under the gate electrode 16B in the region B as shown circled by broken lines in FIG. 10(B). Therefore, especially in a low-voltage operation transistor whose gate length is short, that is, whose gate oxide film 12B is thin, a substantial change in the thickness of the gate oxide film 12B is effected right under the gate electrode 16B, thus causing a problem that a threshold characteristic shifts from a desired value.

[0023]

Indeed, such a problem is prevented from occurring if the protection oxide film 18 is not formed. However, without formation of the protection oxide film 18, electrons retained in the amorphous silicon pattern 13A are dissipated to the sidewall insulating films 16s formed by CVD and etchback as shown in FIG. 11(B) so that information stored in the flash memory device is lost in a short period of time. On the other hand, with a high-quality thermal oxide film 18 hardly allowing a leakage current being formed on the sidewalls of the floating gate electrode pattern 13A, the electrons injected into the floating gate electrode pattern 13 are stably retained therein as shown in FIG. 11(A).

[0024]

Therefore, it is essential to form the protection oxide film 18 in the semiconductor integrated circuit device including the flash memory device. However, formation of

such a protection oxide film inevitably causes the problem of a change in the threshold characteristic of a MOS transistor forming a peripheral or logic circuit. Such a problem of a change in the threshold characteristic of the MOS transistor is noticeable when the MOS transistor is a high-speed transistor having a short gate length.

[0025]

FIG. 12 is a plan view of a configuration of a flash memory cell having a single-layer gate electrode structure by related art.

[0026]

According to FIG. 12, a device region 11A is formed on the Si substrate 11 by a field oxide film 11F. One end of the above-described floating gate electrode pattern 13A is formed on the Si substrate 11 to cross the device region 11A. In the device region 11A, by using the floating gate electrode pattern 13A as a self-alignment mask, the n^--type source region 11a and the n^+-type source line region 11b are formed on one side, and the n^+-type drain region 11c is formed on the other side.

[0027]

On the Si substrate 11, another device region 11B is formed next to the device region 11A. An n^+-type diffusion region 11C is formed in the device region 11B. The other end of the floating gate electrode pattern 13A is formed as a coupling part 13Ac covering the diffusion region 11C.

[0028]

FIG. 13(A) is a sectional view of the flash memory cell of FIG. 12 taken along the line X-X'.

[0029]

According to FIG. 13(A), the tunnel oxide film 12A is formed between the source line region 11b and the drain region 11c on the Si substrate 11, and the floating gate electrode pattern 13A is formed on the tunnel oxide film 12A. Further, the n^--type source region 11a is formed outside the n^+-type source line region 11b in the Si substrate 11. The sidewall insulating films 16s are formed on the sidewalls of the floating gate electrode pattern 13A.

[0030]

FIG. 13(B) is a sectional view of the flash memory cell of FIG. 12 taken along the line y-y'.

[0031]

According to FIG, 13(B), the floating gate electrode pattern 13A continuously extends from the device region 11A having the flash memory cell of FIG. 13 (A) to the adjacent device region 11AC on the field oxide film 11F formed on the Si substrate 11. The coupling part 13Ac of the floating gate electrode pattern 13A is capacitive-coupled via an oxide film 12Ac to the high-density diffusion region 11C.

[0032]

At the time of a write (program) operation, by providing the source line region 11b, applying a drain voltage of +5 V to the drain region 11c, and applying a write voltage of +10 V to the high-density diffusion region 11C as shown in FIGS. 14(A) and 14(B), the potential of the floating gate electrode pattern 13A rises so that hot electrons are injected into the floating gate electrode pattern 13A via the tunnel oxide film 12A in the device region 11A.

[0033]

On the other hand, at the time of an erase operation, an erase voltage of +15 V is applied to the source line region 11b with the drain region 11c and the high-density diffusion region 11C being grounded as shown in FIGS. 14(C) and 14(D). As a result, the electrons in the floating gate electrode pattern 13A tunnel through the tunnel oxide film 12A to the source region 11a to be absorbed into a source power supply through the source line region 11b.

[0034]

Thus, in the flash memory cell of FIG. 12, the high-density diffusion region 11C serves as a control gate electrode, and unlike the conventional flash memory cell of a multilayer gate structure, it is unnecessary to form the above-described ONO insulating film 14 between the polysilicon floating gate electrode and the polysilicon control gate electrode. In the flash memory of FIG. 31, the oxide film 12Ac serves as the ONO insulating film 14. Since the oxide film 12Ac is formed on the Si substrate 11 by thermal oxidation, the oxide film 12Ac has high quality.

[0035]

FIGS. 15(A) through21(M) are diagrams showing a production process of a semiconductor integrated circuit device including the flash memory cell of FIG. 12 in addition to the low-voltage operation transistor B and the high-voltage operation transistor C. In the drawings, the same elements as those previously described are referred to by the same numerals, and a description thereof will be omitted.

[0036]

According to FIG. 15(A), the thermal oxide film 12C of a thickness of 5 to 50 nm is formed on the Si substrate 11 by performing thermal oxidation at temperatures ranging from 800 to 1100 °C in each of the flash memory cell region A, the low-voltage operation transistor region B, and the high-voltage operation transistor region C. In the step of FIG. 15(B), the thermal oxide film 12C is removed from the flash memory cell region A by a patterning process using a resist pattern 15_1.

[0037]

Next, in the step of FIG. 16(C), the resist pattern 15_1 is removed, and the tunnel oxide film 12A of a thickness of 5 to 15 nm is formed on the surface of the Si substrate 11 in the region A by performing thermal oxidation at temperatures ranging from 800 to 1100 °C. In the step of FIG. 16(C), as a result of the thermal oxidation for forming the tunnel oxide film 12A, the thermal oxide film 12C is developed in each of the regions B through D.

[0038]

Next, in the step of FIG. 16(D), the thermal oxide film 12C is removed from the low-voltage operation transistor region B by a patterning process using a resist pattern 152. Then, in the step of FIG. 17(E), after the resist pattern 152 is removed, the thermal oxide film 12B of a thickness of 3 to 10 nm is formed in the region B by performing thermal oxidation at temperatures ranging from 800 to 1100 °C. In the step of FIG. 17(E), as a result of the thermal oxidation for forming the thermal oxide film 12B, the tunnel oxide film 12A is developed in the region A and the thermal oxide film 12C is developed in the region C.

[0039]

Next, in the step of FIG. 17(F), the amorphous silicon film 13 uniformly doped with p and having a thickness of 150 to 200 nm is formed on the Si substrate 11. In the step of FIG. 18(G), patterning is performed on the amorphous silicon film 13 with a resist pattern 17_1, serving as a mask, so that the floating gate electrode pattern 13A is formed in the flash memory cell region A, a gate electrode pattern 13B is formed in the low-voltage operation transistor region B, and a gate electrode pattern 13C is formed in the high-voltage operation transistor region C.

[0040]

Next, in the step of FIG. 18(H), the surfaces of the floating gate electrode pattern 13A and the gate electrode patterns 13B through 13D are covered with the thermally-oxidized film 18 of a thickness of 5 to 10 nm by thermal oxidation at temperatures ranging from 800 to 900 °C. Then, in the step of FIG. 19(I), with a resist pattern 17_2 serving as a mask, the source region 11a is formed by performing ion implantation of p^+ or As^+ with a dose of 1×10^{14} to 5×10^{14} cm^{-2} at accelerating voltages ranging from 30 to 80 keV.

[0041]

Further, in the step of FIG. 19(J), with the regions B and C being covered with a resist pattern 17_3, ion implantation of As^+ is performed with a dose of 5×10^{14} to 3×10^{15} cm^{-2} at accelerating voltages ranging from 30 to 50 keV in the region A by using the floating gate electrode pattern 13A as a self-alignment mask. Thereby, the n^+-type source line region 11b is formed inside the source region 11a

and the n^+-type drain region 11c is formed on the opposite side of a channel region from the source region 11a.

[0042]

Next, in the step of FIG. 20(K), a resist pattern 17_3 covering the flash memory cell region A is formed, and the LDD regions 11d and 11e are formed in the regions B and C, respectively, by ion implantation of a p-type or n-type impurity element.

[0043]

Further, in the step of FIG. 20(L), the sidewall oxide films 16s are formed on both sidewalls of each of the floating gate electrode pattern 13A and the gate electrode patterns 13B and 13C. In the step of FIG. 21(M), with the flash memory region A being covered with a resist pattern 17_4, the diffusion regions 11f and 11g are formed in the regions B and C, respectively, by ion implantation of a p-type or n-type impurity element.

[0044]

Also in the production of the flash memory device of such a single-layer gate structure, when the thermal oxide film 18 is formed as a protection insulating film to cover the single-layer gate electrode structure 13A in the flash memory cell region A as shown in detail in FIG. 22(A) in the step of FIG. 18(H), the same thermal oxide film 18 is also formed in the low-voltage transistor region B so as to cover the gate electrode 13B as shown in FIG. 22(B). As a result, bird's beaks that penetrate right under the gate electrode 13B are formed as shown circled in FIG. 22(B). Therefore, the low-voltage operation transistor formed in the region B is prevented from having a desired threshold characteristic.

[0045]

It is a general object of the present invention to provide a semiconductor device and a method of producing the same in which the above-described disadvantage is eliminated.

[0046]

A more specific object of the present invention is to provide a method of producing a semiconductor device in which a semiconductor circuit integrated device including a flash memory device is formed on a substrate, wherein formation of bird's beak right under the gate electrode of another semiconductor device formed together with the flash memory device on the substrate can effectively be prevented.

[0047]

[Means to Solve the Problems]

According to one aspect of the present invention, the above objects are solved by a semiconductor integrated circuit device comprising: a substrate; a nonvolatile memory device formed in a memory cell region of the substrate; and a semiconductor device formed in a device region of the substrate, the nonvolatile memory device having a multilayer gate electrode structure including a tunnel insulating film covering the surface of the substrate in the memory cell region, a floating gate electrode formed on the tunnel insulating film, an insulating film formed on the floating gate electrode, and a control gate electrode formed on the insulating film, the semiconductor device including a gate insulating film covering the surface of the substrate in the device region and a gate electrode formed on the gate insulating film, the floating gate electrode having sidewall

surfaces covered with a protection insulating film formed of a thermal oxide film, wherein a bird's beak structure, which is formed of a thermal oxide film and penetrates into the floating gate electrode along an interface from the sidewall surfaces of the floating gate electrode, is formed at the interface of the tunnel insulating film and the floating gate electrode, and gate insulating film is interposed between the surface of the substrate and the undersurface of the gate electrode to have a substantially uniform thickness.

[0048]

According to another aspect of the present invention, the above objects are solved by a semiconductor integrated circuit device comprising: a substrate; a nonvolatile memory device formed in a memory cell region of the substrate; and a semiconductor device formed in a device region of the substrate, the nonvolatile memory device including a first active region formed in the memory cell region and covered with a tunnel insulating film, a second active region formed next to the first active region and covered with an insulating film in the memory cell region, a control gate formed of an embedded diffusion region formed in the second active region, a first gate electrode extending on the tunnel insulating film in the first active region and forming a bridge between the first and second active regions in the memory cell region to be capacitive-coupled via the insulating film and the embedded diffusion region in the second active region, and a pair of diffusion regions formed on each of sides of the first gate electrode in the first active region, the semiconductor device being formed of a gate insulating film covering the surface of the substrate in the device region and a second gate electrode formed on the gate insulating film, the first gate electrode having side wall

surfaces thereof covered with a protection insulating film formed of a thermal oxide film, wherein a bird's beak structure, which is formed of a thermal oxide film and penetrates into the first gate electrode along an interface from the sidewall surfaces of the first gate electrode, is formed at the interface of the tunnel insulating film and the first gate electrode, and the gate oxide film is interposed between the surface of the substrate and the undersurface of the second gate electrode to have a substantially uniform thickness.

[0049]

According to still another aspect of the present invention, the above objects are solved by a method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of: forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film covering the first silicon film in the memory cell region, a first gate insulating film covering the first device region, and a second gate insulating film covering the second device region and thicker than the first gate insulating film; depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region, the first gate insulating film in the first device region, and the second

gate insulating film in the second device region; forming a multilayer gate electrode structure in the memory cell region by selectively patterning the second silicon film, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the first and second device regions; forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the first and second device regions; forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks; forming first and second gate electrodes in the first and second device regions by patterning the second silicon film; and forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[0050]

According to yet another aspect of the present invention, the above objects are solved by a method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of: forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first gate insulating film covering the first

device region, and a second gate insulating film covering the second device region and thicker than the first gate insulating film; depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region, the first gate insulating film in the first device region, and the second gate insulating film in the second device region; forming a third gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the first and second device regions; forming a protection oxide film so that the protection oxide film covers the third gate electrode in the memory cell region and the surface of the silicon film in the first and second device regions; forming diffusion regions in both sides of the third gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the third gate electrode and the silicon film being employed as masks; forming first and second gate electrodes in the first and second device regions by patterning the silicon film; and forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[0051]

According to yet another aspect of the present invention, the above objects are solved by a method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate where the memory cell region and the logic device region are defined, the method comprising the steps of: forming a semiconductor structure including a tunnel insulating film covering the memory cell

region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film covering the first silicon film in the memory cell region, and a gate insulating film covering the logic device region; depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region and the gate insulating film in the logic device region; forming a multilayer gate electrode structure in the memory cell region by selectively patterning the second silicon film to be a control gate electrode, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the logic device region; forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the logic device region; forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks; forming gate electrodes in the logic device region by patterning the second silicon film; and forming diffusion regions in the logic device region by performing ion implantation with the gate electrodes being employed as masks.

[0052]

According to yet another aspect of the present invention, the above problems are solved by a method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate where the memory cell

region and the logic device region are defined, the method comprising the steps of: forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate and a gate insulating film covering the logic device region; depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region and the gate insulating film in the logic device region; forming a first gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the logic device region; forming a protection oxide film so that the protection oxide film covers the first gate electrode in the memory cell region and the surface of the silicon film in the logic device region; forming diffusion regions in both sides of the first gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the first gate electrode and the silicon film being employed as masks; forming a second gate electrode in the logic device region by patterning the silicon film; and forming diffusion regions in the logic device region by performing ion implantation with the second gate electrode being employed as a mask.

[Operation]

According to the present invention, a protection oxide film is formed to cover a multilayer gate electrode structure or a floating gate electrode pattern in a nonvolatile memory cell region before a gate electrode is patterned in a first or second device region. The protection oxide film prevents a bird' beak structure from being formed to penetrate into the gate electrode in the device region. Therefore, the problem of a change in the threshold characteristic of a semiconductor device in the device region

can be avoided. Further, according to the present invention, when diffusion regions are formed in the nonvolatile memory cell region by ion implantation, the device region is covered with a silicon film. By using the silicon film as a mask, a resist process may be omitted.

[0053]

[Embodiments of the Invention]

[FIRST EMBODIMENT]

FIGS. 23(A) through 27(I) are diagrams showing a production process of a semiconductor integrated circuit device according to a first embodiment of the present invention. In the drawings, the same elements as those previously described are referred to by the same numerals, and a description thereof will be omitted.

[0054]

In this embodiment, the steps of FIGS. 1(A) through 4(G) are first performed, so that a structure corresponding to FIG. 4(G) is obtained in the step of FIG. 23(A). At this point, a silicon-on-insulator (SOI) substrate may replace the Si substrate 11. Further, a tunnel nitride film may replace the tunnel oxide film 12A.

[0055]

Further, in the step of FIG. 23(B), the multilayer gate electrode structure 16F is formed in the flash memory cell region A by performing patterning using the resist pattern 17A described in the step of FIG. 4(H). In the step of FIG. 23(B), no patterning is performed on the low-voltage operation transistor region B and the high-voltage operation transistor region C that are covered with the resist pattern 17A.

[0056]

In this embodiment, next, in the step of FIG. 24(C), the resist pattern 17A is removed, and the protection insulating film 18 is formed of a thermal oxide film to cover the multilayer gate electrode structure 16F by performing thermal oxidation at temperatures ranging from 800 to 900 °C. The same thermal oxide film 18 is also formed on the surface of the amorphous silicon film 16 in each of the regions B and C.

[0057]

Further, in the step of FIG. 24(C), with the multilayer gate electrode structure 16F serving as a self-alignment mask, the diffusion region 11c is formed in the flash memory cell region A by performing ion implantation of As^+ (or p^+) under the same conditions as in the above-described step of FIG. 6(L). The concentration may be the same on the side of the diffusion regions 11a and 11b and the side of the diffusion region 11c. At this point, no ion is injected into the Si substrate 11 in the regions B and C that are covered with the amorphous silicon film 16. A resist pattern that has an opening on the flash memory cell region A may be employed.

[0058]

In the step of FIG. 24(D), by using the resist pattern 17B previously described in the step of FIG. 5(I) as a mask, patterning is performed on the amorphous silicon film 16 in the regions B and C so that the gate electrodes 16B and 16C are formed in the low-voltage operation transistor region B and the high-voltage operation transistor region C, respectively.

[0059]

Next, in the step of FIG. 25(E), with the resist pattern 19C previously described in the step of FIG. 7(M) being employed as a mask, the LDD diffusion regions 11d are formed in the Si substrate 11 in the region B by performing ion implantation of an n-type or p-type impurity element therein.

[0060]

In the step of FIG. 25(F), with the resist pattern 19D previously described in the step of FIG. 7(N) being employed as a mask, the LDD diffusion regions 11e are formed in the Si substrate 11 in the region C by performing ion implantation of an n-type or p-type impurity element therein. In the steps of FIGS. 9(E) and 9(F), the diffusion regions 11d and 11e may be formed under the same ion implantation conditions in the same step.

[0061]

In the step of FIG. 26(G), which corresponds to the above-described step of FIG. 8(O), the sidewall insulating films 16s are formed on each of the multilayer gate electrode structure 16F and the gate electrodes 16B and 16C. In the step of FIG. 26(H), which corresponds to the above-described step of FIG. 8(P), the flash memory cell region A is covered with the resist pattern 19E. Further, in the step of FIG. 26(H), with the gate electrodes 16B and 16C and the sidewall insulating films 16s being used as self-alignment masks, the diffusion regions 11f is formed in the Si substrate 11 in the regions B and C, respectively, by performing ion implantation of an n-type or p-type impurity element therein.

[0062]

Further, by performing the same step as previously described in FIG. 9(Q), a semiconductor integrated circuit device of the structure of FIG. 27(I) corresponding to FIG. 9(Q) can be obtained.

[0063]

In this embodiment, when the protection insulating film 18 is formed by thermal oxidation in the step of FIG. 24(C), no patterning has been performed on the amorphous silicon film 16 in the regions B and C. As a result, in the regions B and C, the thermal oxide film 18 is formed on the surface of the amorphous silicon film 16, but is prevented from being formed at an interface between the amorphous silicon film 16 and the gate oxide film 12B. Further, no such thermal oxidation is performed in any step after the patterning step of the gate electrodes 16B and 16C of FIG. 24(D). Therefore, although the protection insulating film 13 is formed to cover the multilayer gate electrode structure 16F as shown circled in FIG. 28(A), no thermal oxide film other than the gate oxide film 12B is developed on the bottom of the gate electrode 16B. Therefore, the problem of a change in the threshold characteristic of the low-voltage operation transistor can be avoided.

[0064]

As shown circled in FIG. 28(A), in the step of FIG. 24(C), bird's beaks are formed under the floating gate electrode pattern 13A with the formation of the protection insulating film 13. On the other hand, with respect to the MOS transistors of the regions B and C, bird's beaks, if ever formed, are far smaller in thickness and penetration distance

than those formed under the floating gate electrode pattern 13A.

[0065]

Further in this embodiment, as shown in FIGS. 29(A) and 29(B), in the ion implantation step of FIG. 24(C), no resist pattern is required to be provided in the low-voltage operation transistor region B and the high-voltage operation transistor region C since the regions B and C are covered with the amorphous silicon film 16. Consequently, this simplifies the production process of the semiconductor integrated circuit device.

[SECOND EMBODIMENT]

FIGS. 30(A) through 34(I) are diagrams showing a production method of a semiconductor integrated circuit device including a flash memory device of a single-layer gate electrode structure according to a second embodiment of the present invention. In the drawings, the same elements as those previously described are referred to by the same numerals, and a description thereof will be omitted.

[0066]

In this embodiment, steps corresponding to those of FIGS. 15(A) through 16(D) are first performed, so that a structure corresponding to that of FIG. 17(E) is obtained in the step of FIG. 30(A). In this embodiment, an SOI substrate may also replace the Si substrate 11. Further, a thermal nitride oxide film may replace the tunnel oxide film 12A or the thermal oxide films 12B and 12C.

[0067]

Next, in the step of FIG. 30(B), which corresponds

to the step of FIG. 17(F), the amorphous silicon film 13 of a thickness of 100 to 300 nm is deposited on the structure of FIG. 30(A). The amorphous silicon film 13 may be replaced by a polysilicon film. Further, the amorphous silicon film 13 may be doped with p^+. In the step of FIG. 31(C), patterning is performed on the amorphous silicon film 13 by using a resist pattern 27_1 as a mask so that the floating gate electrode pattern 13A is formed. The resist pattern 27_1 covers the low-voltage operation transistor region B and the high-voltage operation transistor region C. Consequently, no patterning is performed on the amorphous silicon film 13 in the regions B and C in the step of FIG. 30(B).

[0068]

Next, in the step of FIG. 31(D), the resist pattern 27_1 is removed, and the protection insulating film 18 of a thickness of 5 to 10 nm is formed of a thermal oxide film so as to cover the floating gate electrode pattern 13A in the region A by performing thermal oxidation at temperatures ranging from 800 to 900 °C. As a result of the thermal oxidation, the thermal oxide film 18 is also formed on the surface of the amorphous silicon film 13 in the regions B and C.

[0069]

Next, in the step of FIG. 32(E), a resist pattern 27_2 corresponding to the resist pattern 17_2 in FIG. 19(I) is formed on the structure of FIG. 31(D). With the resist pattern 27_2 being employed as a mask, ion implantation of p^+ (or As^+) is performed with a dose of 1×10^{14} to 5×10^{14} cm^{-2} at accelerating voltages ranging from 30 to 80 keV so that the diffusion region 11a is formed next to the floating gate electrode pattern 13A in the flash memory cell region A.

Further in the step of FIG. 32(E), after the ion implantation of p^+, ion implantation of As^+ is performed with a dose of 1×10^{15} to 6×10^{15} cm^{-2} at accelerating voltages ranging from 30 to 80 keV so that the resistance of the diffusion region 11a is reduced.

[0070]

Next, in the step of FIG. 32(F), the resist pattern 27_2 is removed, and with the floating gate electrode pattern 13A being employed as a mask, ion implantation of As^+ (or P^+) is performed with a dose of 5×10^{14} to 3×10^{15} cm^{-2} at accelerating voltages ranging from 20 to 60 keV in the region A so that the diffusion regions 11b and 11c are formed in the Si substrate 11 in the region A. At this point, the step of FIG. 32(E) is omittable. Further, a resist pattern having an opening only on the flash memory cell region may be formed alternatively.

[0071]

Next, in the step of FIG. 33(G), a resist pattern 27_3 is formed on the structure of FIG. 32(F). The flash memory cell region A is covered with the resist pattern 27_3. Then, patterning is performed on the amorphous silicon film 13 with the resist pattern 27_3 being employed as a mask in the regions B and C so that the gate electrodes 13B and 13C are formed therein.

[0072]

In the step of FIG. 33(H), a resist pattern 27_4 covering the flash memory cell region A is formed. With the resist pattern 27_4 being employed as a mask, an n-type or p-type impurity element is introduced into the Si substrate 11 by ion implantation so that the LDD diffusion regions 11d

and 11e are formed in the regions B and C, respectively.

[0073]

Further, in the step of FIG. 34(I), the resist pattern 27_4 is removed, and a CVD oxide film 16S is deposited. Further, with the CVD oxide film 16S being protected by a resist pattern 27_5 in the flash memory cell region A, etchback is performed in the regions B and C so that the sidewall oxide films 16s are formed on the sidewalls of each of the gate electrodes 13B and 13C.

[0074]

Furthermore, by performing the same ion implantation as in the step of FIG. 21(M) on the structure of FIG. 34(I), the diffusion regions 11f and 11g are formed in the Si substrate 11. A p-type or n-type gate electrode is also formable.

[0075]

FIGS. 35(A) and 35(B) are diagrams showing detailed configurations of the flash memory device and the low-voltage operation transistor formed according to this embodiment.

[0076]

As shown in FIG. 35(A), the floating gate electrode pattern 13A has not only its sidewall faces but also its top surface uniformly covered with the protection insulating film 18 in this embodiment. Therefore, electrons accumulated in the floating gate electrode pattern 13A are stably retained even if the flash memory device is left in a hot environment for a long time.

[0077]

Further in this embodiment, the amorphous silicon film 13 is not patterned in the regions B and C when the thermal oxidation step of FIG. 31(D) is performed. Therefore, as shown in FIGS. 35(B), no bird' beaks of the thermal oxide film penetrate under the gate electrodes 13B and 13C. This stabilizes the threshold characteristic and the operation characteristic of each MOS transistor formed on the Si substrate 11 on which the flash memory device is formed as well. The improvements in the threshold characteristic and the operation characteristic are remarkable in a low-voltage operation transistor having a short gate length and a thin gate oxide film.

[0078]

In this embodiment, no resist pattern is required to be formed in the ion implantation step of FIG. 32(F), thus simplifying the production process.

[0079]

In the flash memory device of a multilayer-gate type according to the previous embodiment, the multilayer gate electrode structure 16F may also have its sidewall faces and top surface covered continuously with the protection insulating film 18 in the configuration of FIG. 7(I) as in that of FIG. 34(I).

[0080]

The present invention is not limited to the specifically disclosed embodiments, but variations and modifications may be made without departing from the scope of the present invention.

[0081]

(Appendant Note 1)

A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of the substrate; and

a semiconductor device formed in a device region of the substrate,

the nonvolatile memory device having a multilayer gate electrode structure including a tunnel insulating film covering the surface of the substrate in the memory cell region, a floating gate electrode formed on the tunnel insulating film, an insulating film formed on the floating gate electrode, and a control gate electrode formed on the insulating film,

the semiconductor device including a gate insulating film covering the surface of the substrate in the device region and a gate electrode formed on the gate insulating film,

the floating gate electrode having sidewall surfaces covered with a protection insulating film formed of a thermal oxide film, wherein

a bird's beak structure, which is formed of a thermal oxide film and penetrates into the floating gate electrode along an interface from the sidewall surfaces of the floating gate electrode, is formed at the interface of the tunnel insulating film and the floating gate electrode, and

gate insulating film is interposed between the surface of the substrate and the undersurface of the gate electrode to have a substantially uniform thickness.

(Appendant Note 2)

A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of the substrate; and

a semiconductor device formed in a device region of the substrate,

the flash memory device including

a first active region formed in the memory cell region and covered with a tunnel insulating film, a second active region formed next to the first active region and covered with an insulating film in the memory cell region, a control gate formed of an embedded diffusion region formed in the second active region, a first gate electrode extending on the tunnel insulating film in the first active region and forming a bridge between the first and second active regions in the memory cell region to be capacitive-coupled via the insulating film and the embedded diffusion region in the second active region, and a pair of diffusion regions formed on each of sides of the first gate electrode in the first active region,

the semiconductor device being formed of a gate insulating film covering the surface of the substrate in the device region and a second gate electrode formed on the gate insulating film,

the first gate electrode having side wall surfaces thereof covered with a protection insulating film formed of a thermal oxide film, wherein

a bird's beak structure, which is formed of a thermal oxide film and penetrates into the first gate electrode along an interface from the sidewall surfaces of the first gate electrode, is formed at the interface of the tunnel insulating film and the first gate electrode, and

the gate oxide film is interposed between the surface of the substrate and the undersurface of the second gate electrode to have a substantially uniform thickness.

[0082]

(Appendant Note 3)

The semiconductor integrated circuit device as claimed in appendant note 1 or 2, wherein the thermal oxide film forming the protection insulating film connects to the bird's beak structure.

[0083]

(Appendant Note 4)

The semiconductor integrated circuit device as claimed in appendant note 1 or 2, wherein the protection insulating film continuously covers the top surface of the first gate electrode.

[0084]

(Appendant Note 5)

The semiconductor integrated circuit device as claimed in appendant note 1 or 3, wherein each of the gate electrode and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

[0085]

(Appendant Note 6)

The semiconductor integrated circuit device as claimed in any one of appendant notes 2 through 4, wherein the second gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or

p-type dopant.

[0086]

(Appendant Note 7)

The semiconductor integrated circuit device as claimed in any one of appendant notes 1 through 6, wherein a silicon-on-insulator substrate is employed as the substrate.

[0087]

(Appendant Note 8)

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film covering the first silicon film in the memory cell region, a first gate insulating film covering the first device region, and a second gate insulating film covering the second device region and thicker than the first gate insulating film;

depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region, the first gate insulating film in the first device region, and the second gate insulating film in the second device region;

forming a multilayer gate electrode structure in

the memory cell region by selectively patterning the second silicon film to be a control gate electrode, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the first and second device regions;

forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the first and second device regions;

forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks;

forming first and second gate electrodes in the first and second device regions by patterning the second silicon film; and

forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[0088]

(Appendant Note 9)

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate where the memory cell region and the logic device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first silicon film covering the tunnel insulating film in the memory cell region, an insulating film

covering the first silicon film in the memory cell region, and a gate insulating film covering the logic device region;

depositing a second silicon film on the semiconductor structure so that the second silicon film covers the insulating film in the memory cell region and the gate insulating film in the logic device region;

forming a multilayer gate electrode structure in the memory cell region by selectively patterning the second silicon film to be a control gate electrode, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the logic device region;

forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the surface of the second silicon film in the logic device region;

forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks;

forming gate electrodes in the logic device region by patterning the second silicon film; and

forming diffusion regions in the logic device region by performing ion implantation with the gate electrodes being employed as masks.

[0089]

(Appendant Note 10)

The method of producing a semiconductor integrated circuit device according to appendant note 8, wherein the step of depositing the second silicon film is performed simultaneously in the memory cell region and the

first and second device regions.

[0090]

(Appendant Note 11)

The method of producing a semiconductor integrated circuit device according to appendant note 9, wherein the step of depositing the second silicon film is performed simultaneously in the memory cell region and the logic device regions.

[0091]

(Appendant Note 12)

The method of producing a semiconductor integrated circuit device according to any one of appendant notes 8 through 11, wherein the step of forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region is performed without using a resist mask.

[0092]

(Appendant Note 13)

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region, a first semiconductor device corresponding to a first device region, and a second semiconductor device corresponding to a second device region on a substrate where the memory cell region, the first device region, and the second device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate, a first gate insulating film covering the first device region, and a second gate insulating film covering the

second device region and thicker than the first gate insulating film;

depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region, the first gate insulating film in the first device region, and the second gate insulating film in the second device region;

forming a third gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the first and second device regions;

forming a protection oxide film so that the protection oxide film covers the third gate electrode in the memory cell region and the surface of the silicon film in the first and second device regions;

forming diffusion regions in both sides of the third gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the third gate electrode and the silicon film being employed as masks;

forming first and second gate electrodes in the first and second device regions by patterning the silicon film; and

forming diffusion regions in the first and second device regions by performing ion implantation with the first and second gate electrodes being employed as masks.

[0093]

(Appendant Note 14)

A method of producing a semiconductor integrated circuit device which forms a nonvolatile memory device corresponding to a memory cell region and a semiconductor device corresponding to a logic device region on a substrate

where the memory cell region and the logic device region are defined, the method comprising the steps of:

forming a semiconductor structure including a tunnel insulating film covering the memory cell region of the substrate and a gate insulating film covering the logic device region;

depositing a silicon film on the semiconductor structure so that the silicon film covers the tunnel insulating film in the memory cell region and the gate insulating film in the logic device region;

forming a first gate electrode by selectively patterning the silicon film in the memory cell region with the silicon film being left in the logic device region;

forming a protection oxide film so that the protection oxide film covers the first gate electrode in the memory cell region and the surface of the silicon film in the logic device region;

forming diffusion regions in both sides of the first gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the first gate electrode and the silicon film being employed as masks;

forming a second gate electrode in the logic device region by patterning the silicon film; and

forming diffusion regions in the logic device region by performing ion implantation with the second gate electrode being employed as a mask.

[0094]

(Appendant Note 15)

The method of producing a semiconductor integrated circuit device as claimed in appendant note 13, wherein the step of depositing the amorphous silicon film is

performed simultaneously in the memory cell region and the first and second device regions.

[0095]

(Appendant Note 16)

The method of producing a semiconductor integrated circuit device as claimed in appendant note 14, wherein the step of depositing the silicon film is performed simultaneously in the memory cell region and the logic device region.

[0096]

(Appendant Note 17)

The method of producing a semiconductor integrated circuit device as claimed in any one of appendant notes 8 through 11 or 13 through 16, wherein the step of forming the protection oxide film employs thermal oxidation and the protection oxide film is formed of a thermal oxide film.

[0097]

(Appendant Note 18)

The method of producing a semiconductor integrated circuit device as claimed in appendant note 13, 15, or 17, wherein the step of forming diffusion regions in both sides of the third gate electrodes in the memory cell region is performed without using a resist mask.

[0098]

(Appendant Note 19)

The method of producing a semiconductor integrated circuit device as claimed in any one of appendant notes 8 through 18, wherein the step of ion implanting in the first and second device regions is performed with the memory

cell region being protected by a resist mask.

[0099]

(Appendant Note 20)

The method of producing a semiconductor integrated circuit device as claimed in any one of appendant notes 8 through 19, wherein each of the gate electrode, the first gate electrode, the second gate electrode, and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

[0100]

[Advantage of the Invention]

According to the present invention, a protection oxide film is formed to cover a multilayer gate electrode structure or a floating gate electrode pattern in a flash memory cell region before a gate electrode is patterned in a first or second device region. The protection oxide film prevents a bird' beak structure from being formed to penetrate into the gate electrode in the device region. Therefore, the problem of a change in the threshold characteristic of a semiconductor device in the device region can be avoided. Further, according to the present invention, when diffusion regions are formed in the flash memory cell region by ion implantation, the device region is covered with an amorphous silicon film. By using the amorphous silicon film as a mask, a resist process may be omitted.

[Brief Description of the Drawings]

[FIG. 1] FIGS. 1(A) and 1(B) are diagrams (1) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of

a multilayer gate structure.

[FIG. 2] FIGS. 2(C) and 2(D) are diagrams (2) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 3] FIGS. 3(E) and 3(F) are diagrams (3) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 4] FIGS. 4(G) and (H) are diagrams (4) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 5] FIGS. 5(I) and (J) are diagrams (5) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 6] FIGS. 6(K) and (L) are diagrams (6) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 7] FIGS. 7(M) and (N) are diagrams (7) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 8] FIGS. 8(O) and (P) are diagrams (8) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 9] FIG. 9(Q) is a diagram (8) showing a production process of a conventional semiconductor integrated circuit device including a flash memory device of a multilayer gate structure.

[FIG. 10] FIGS. 10(A) and 10(B) are diagrams for illustrating a disadvantage of the conventional semiconductor integrated circuit device including the flash memory device of the multilayer gate structure.

[FIG. 11] FIGS. 11(A) and 11(B) are diagrams for illustrating a role of a protection oxide film employed in the conventional flash memory device of the multilayer gate structure.

[FIG. 12] FIG. 12 is a plan view of a flash memory device of a single-layer gate structure according to related art of the present invention.

[FIG. 13] FIGS. 13(A) and 13(B) are sectional views of the flash memory device of FIG. 12.

[FIG. 14] FIGS. 14(A) through 14(D) are diagrams for illustrating write and erase operations of the flash memory device of FIG. 12.

[FIG. 15] FIGS. 15(A) and 15(B) are diagrams (1) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 16] FIGS. 16(C) and 16(D) are diagrams (2) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 17] FIGS. 17(E) and 17(F) are diagrams (3) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 18] FIGS. 18(G) and 18(H) are diagrams (4) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 19] FIGS. 19(I) and 19(J) are diagrams (5) showing

a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 20] FIGS. 20(K) and 20(L) are diagrams (6) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 21] FIG. 21(M) is a diagram (7) showing a production process of a semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 22] FIGS. 22(A) and 22(B) are diagrams for illustrating a disadvantage of the semiconductor integrated circuit device including the flash memory device of a single-layer gate structure of FIG. 12.

[FIG. 23] FIGS. 23(A) and 23(B) are diagrams (1) showing a production process of a semiconductor integrated circuit device according to a first embodiment of the present invention.

[FIG. 24] FIGS. 24(C) and 24(D) are diagrams (2) showing a production process of a semiconductor integrated circuit device according to a first embodiment of the present invention.

[FIG. 25] FIGS. 25(E) and 25(F) are diagrams (3) showing a production process of a semiconductor integrated circuit device according to a first embodiment of the present invention.

[FIG. 26] FIGS. 26(G) and 26(H) are diagrams (4) showing a production process of a semiconductor integrated circuit device according to a first embodiment of the present invention.

[FIG. 27] FIG. 27(I) is a diagram (5) showing a production process of a semiconductor integrated circuit device

according to a first embodiment of the present invention.
[FIG. 28] FIGS. 28(A) and 28(B) are diagrams for illustrating an effect of the first embodiment.
[FIG. 29] FIGS. 29(A) and 29(B) are diagrams for illustrating another effect of the first embodiment.
[FIG. 30] FIGS. 30(A) and 30(B) are diagrams (1) showing a production process of a semiconductor integrated circuit device according to a second embodiment of the present invention.
[FIG. 31] FIGS. 31(C) and 30(D) are diagrams (2) showing a production process of a semiconductor integrated circuit device according to a second embodiment of the present invention.
[FIG. 32] FIGS. 32(E) and 32(F) are diagrams (3) showing a production process of a semiconductor integrated circuit device according to a second embodiment of the present invention.
[FIG. 33] FIGS. 33(G) and 33(H) are diagrams (4) showing a production process of a semiconductor integrated circuit device according to a second embodiment of the present invention.
[FIG. 34] FIG. 34(I) is a diagram (5) showing a production process of a semiconductor integrated circuit device according to a second embodiment of the present invention.
[FIG. 35] FIGS. 35(A) and 35(B) are diagrams for illustrating effects of the second embodiment.

[Description of the Reference Numerals]
11: substrate
11a, 11b, 11c, 11d, 11e, 11f: diffusion region
12A: tunnel oxide film
12B, 12C: gate oxide film
13, 16: amorphous silicon film

13A: floating gate electrode

14: ONO insulating film

15A, 15B, 17A, 17B, 19A to 19E: resist pattern

15_1, 15_2: resist pattern

17_1, 17_2, 17_3: resist pattern

16B, 16C: gate electrode

16F: floating gate electrode

16s: sidewall insulating film

18: protection oxide film

[Name of the Document] Abstract

[Abstract]

[Object]

In a semiconductor integrated circuit device including a flash memory device, formation of bird's beak right under a gate electrode of a MOS transistor constituting a logic device is prevented while a floating gate electrode is covered with a protection oxide film.

[Solution Means]

A multilayer gate electrode or single-layer gate of the flash memory device is formed by uniformly depositing an amorphous silicon film on a substrate where a memory cell region and a device region are defined, and patterning the amorphous silicon film in the memory cell region with the device region on the substrate covered with the amorphous silicon film. In this state, the protection oxide film is formed by performing thermal oxidation, followed by patterning the amorphous silicon film to form a gate electrode in the device region.

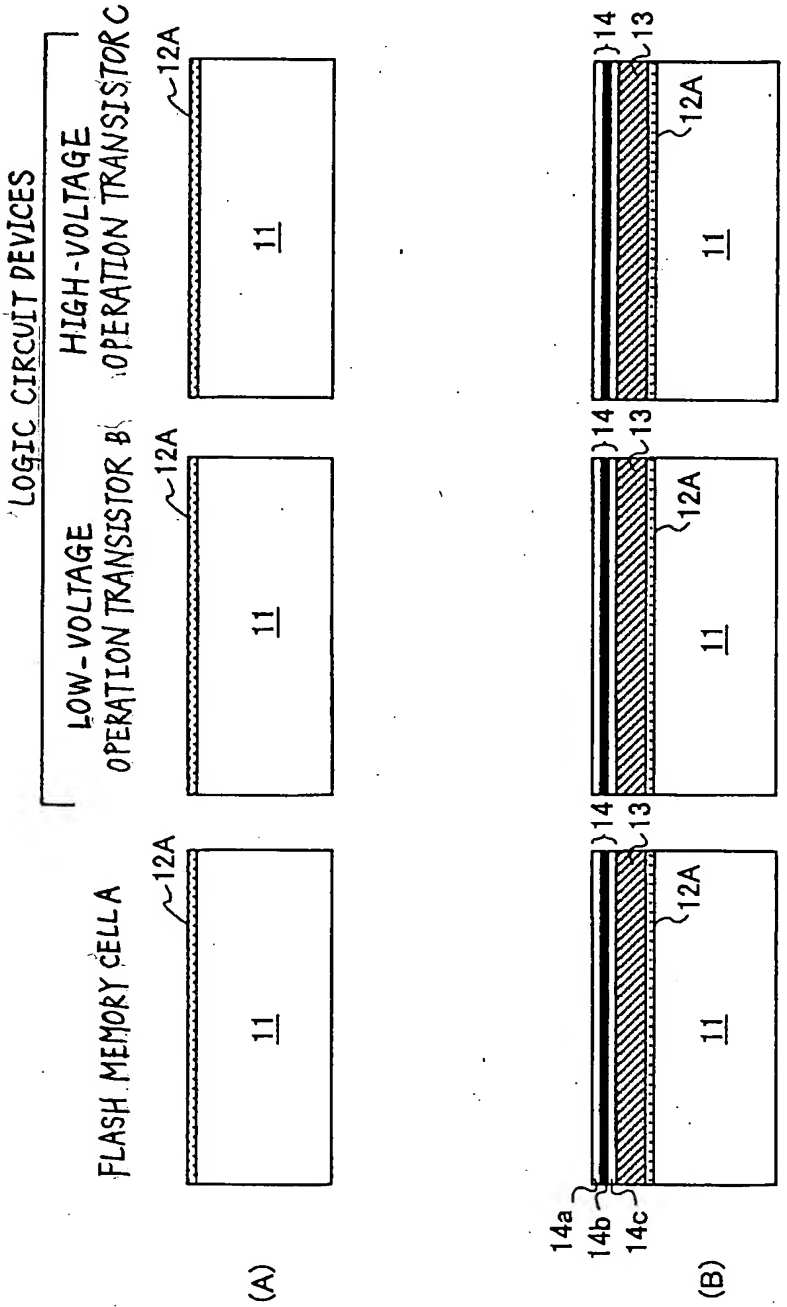
[Selected Figure] FIG. 25

01147

(NAME OF THE DOCUMENT)　DRAWINGS

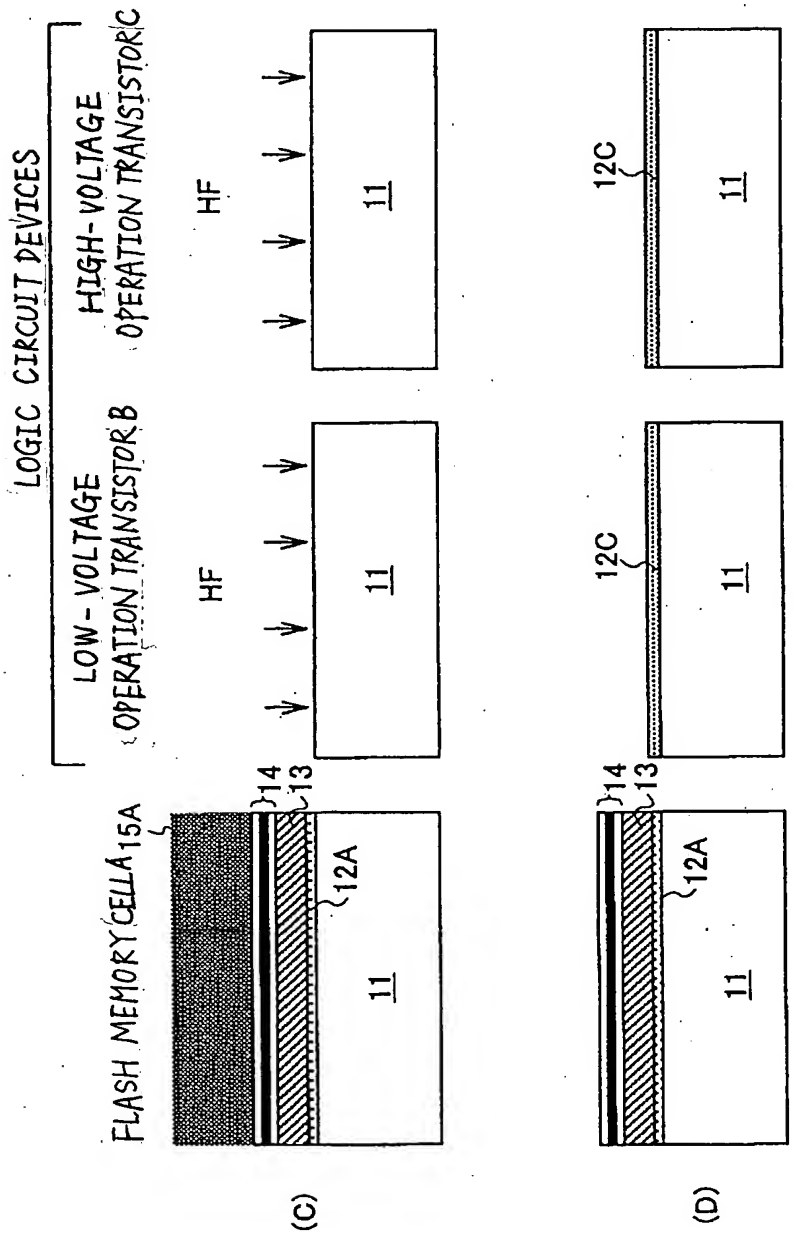
(FIG. 1)

(A) AND (B) ARE DIAGRAMS (1) SHOWING A PRODUCION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED-CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTI LAYER GATE STRUCTURE.



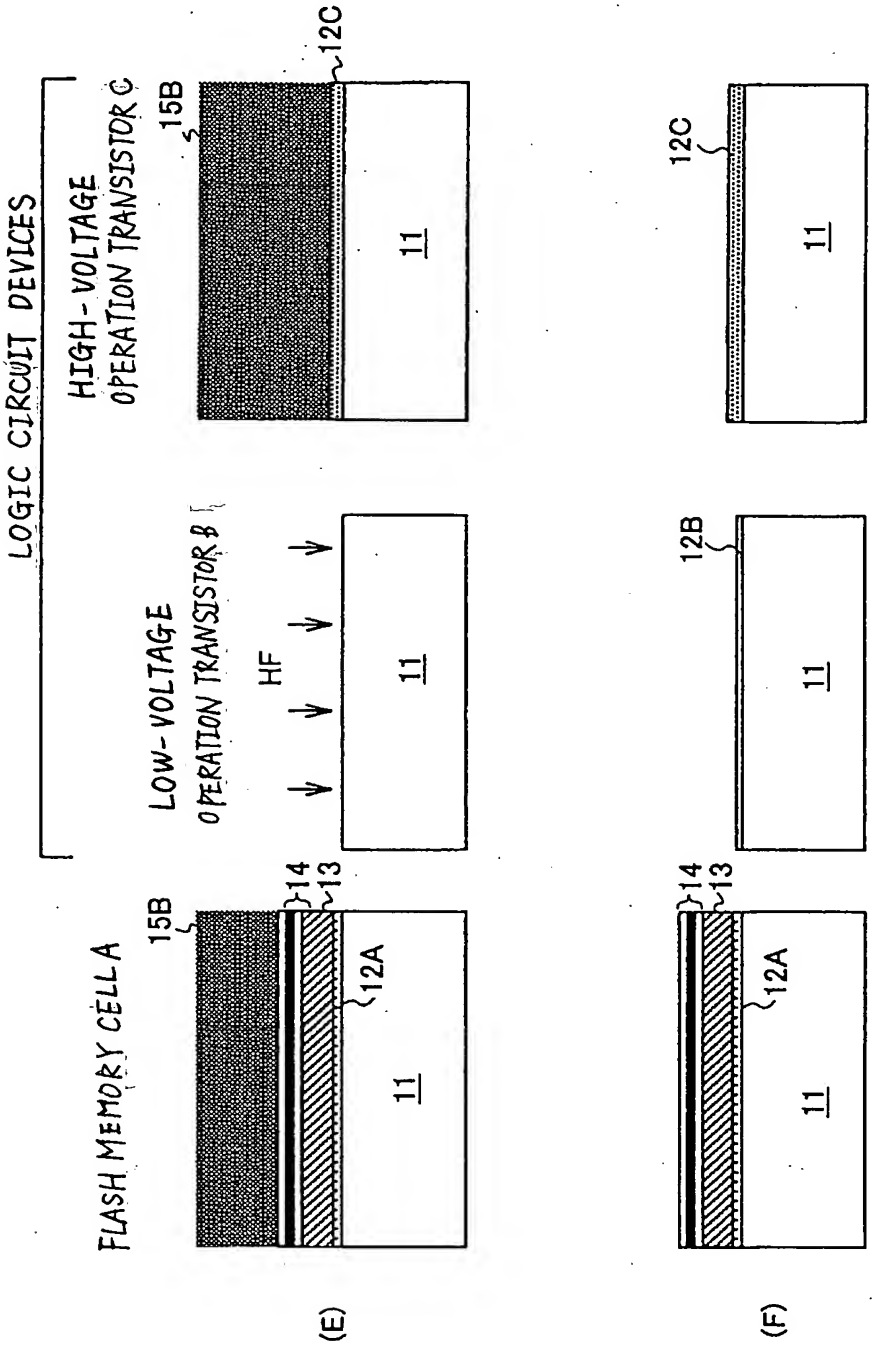
【FIG. 2】

(C) AND (D) ARE DIAGRAMS (2) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



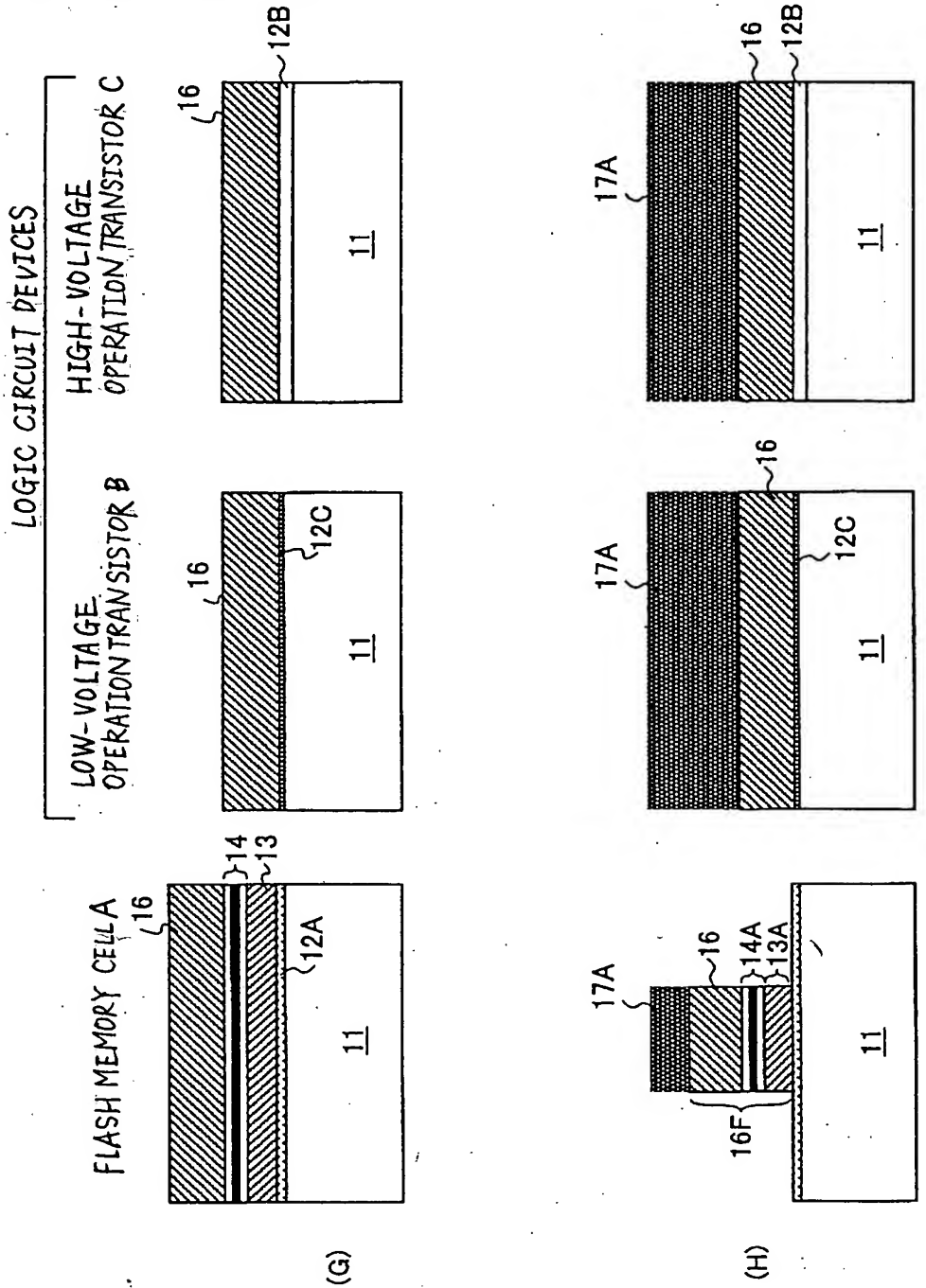
[FIG.3]

(E) AND (F) ARE DIAGRAMS (3) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED-CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



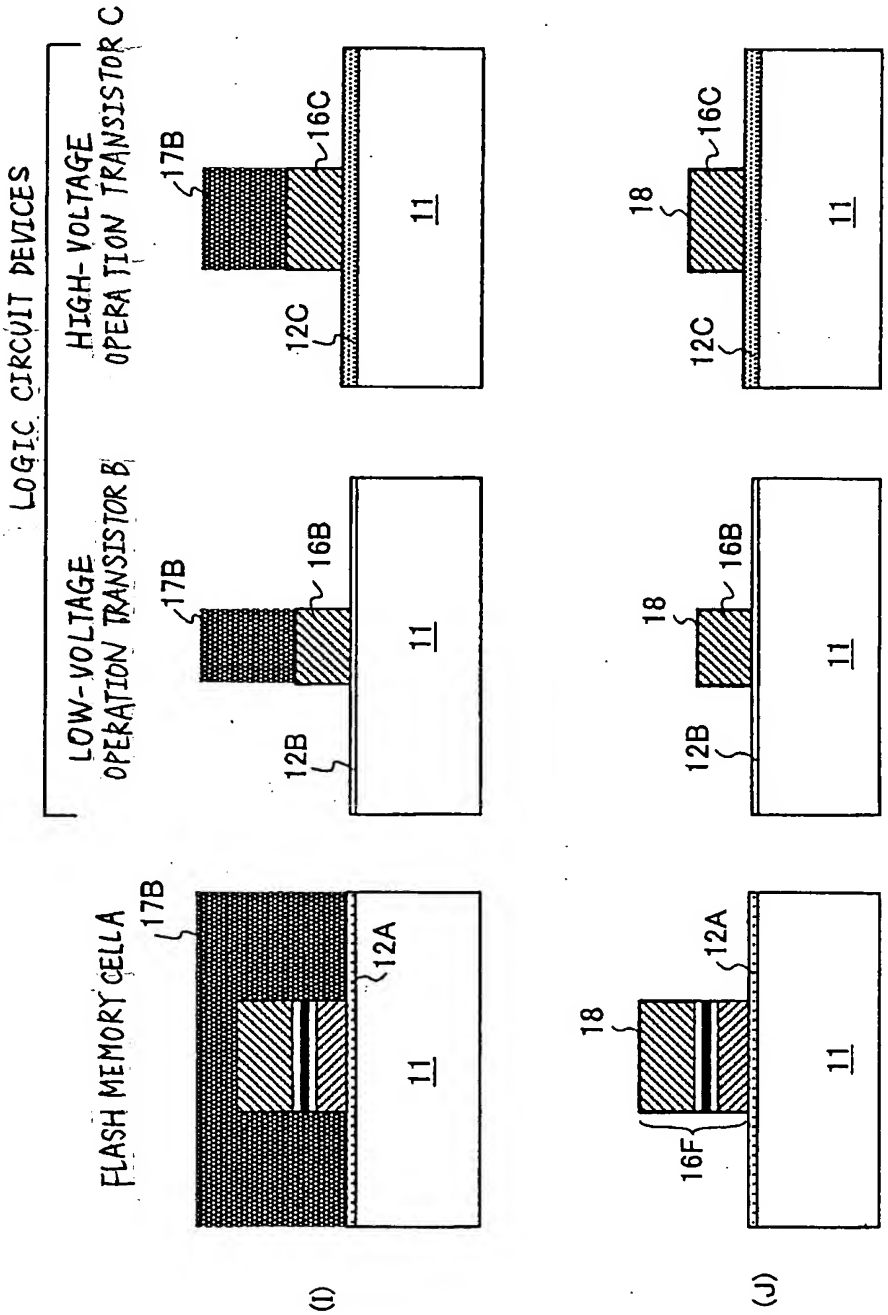
〔FIG.4〕

(G) AND (H) ARE DIAGRAMS (4) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



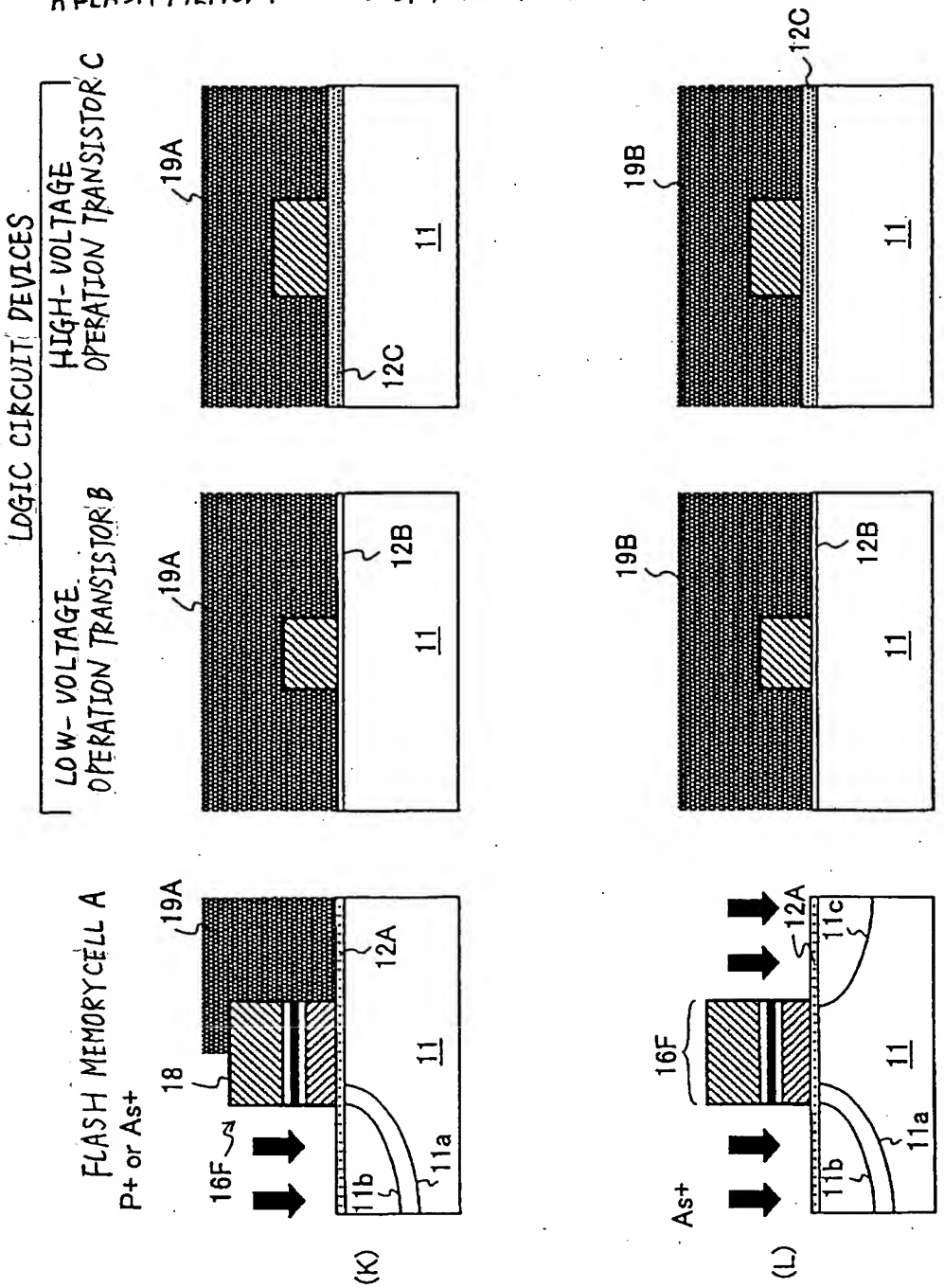
〔FIG.5〕

(I) AND (J) ARE DIAGRAMS (5) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



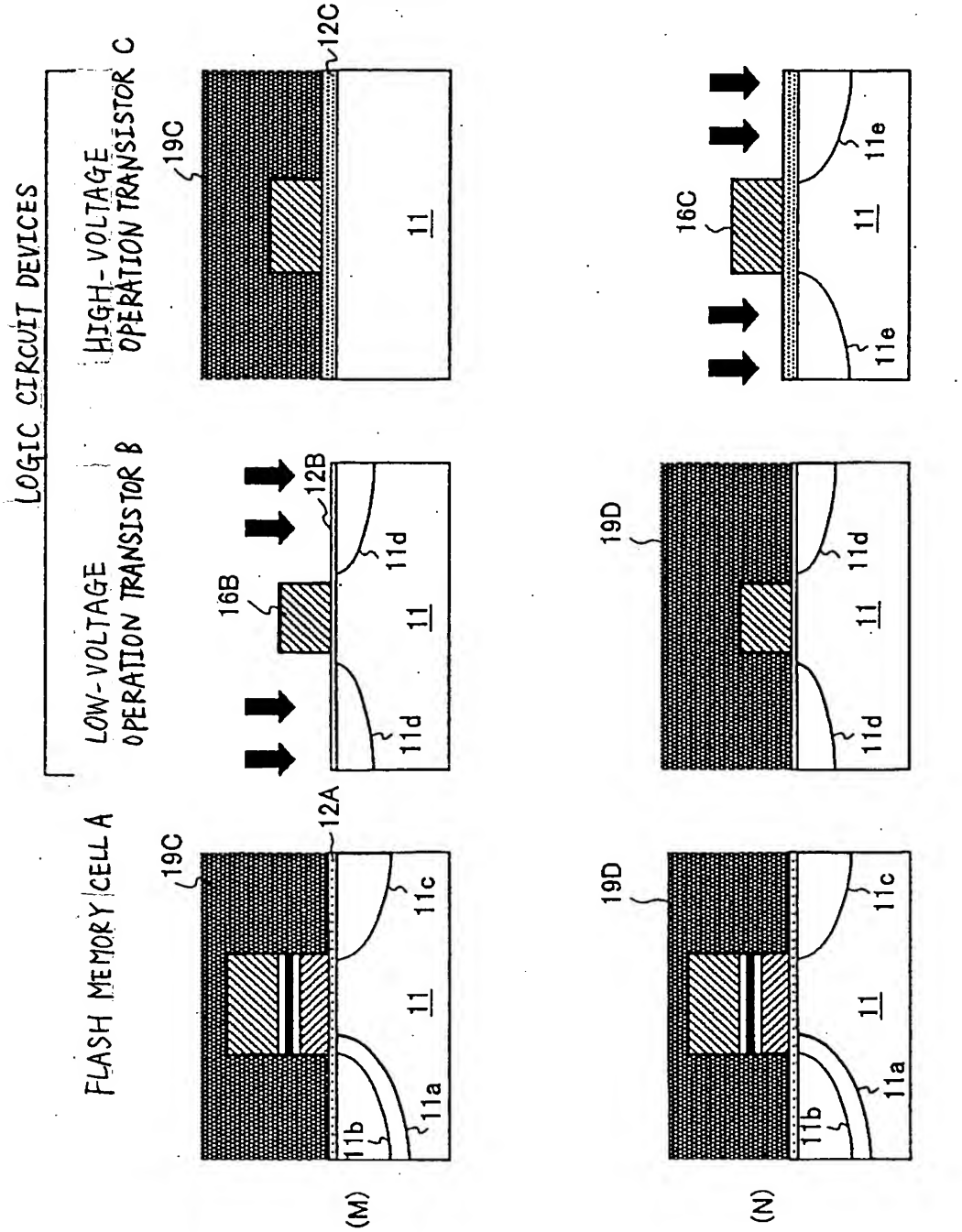
(FIG.6)

(K) AND (L) ARE DIAGRAMS (6) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



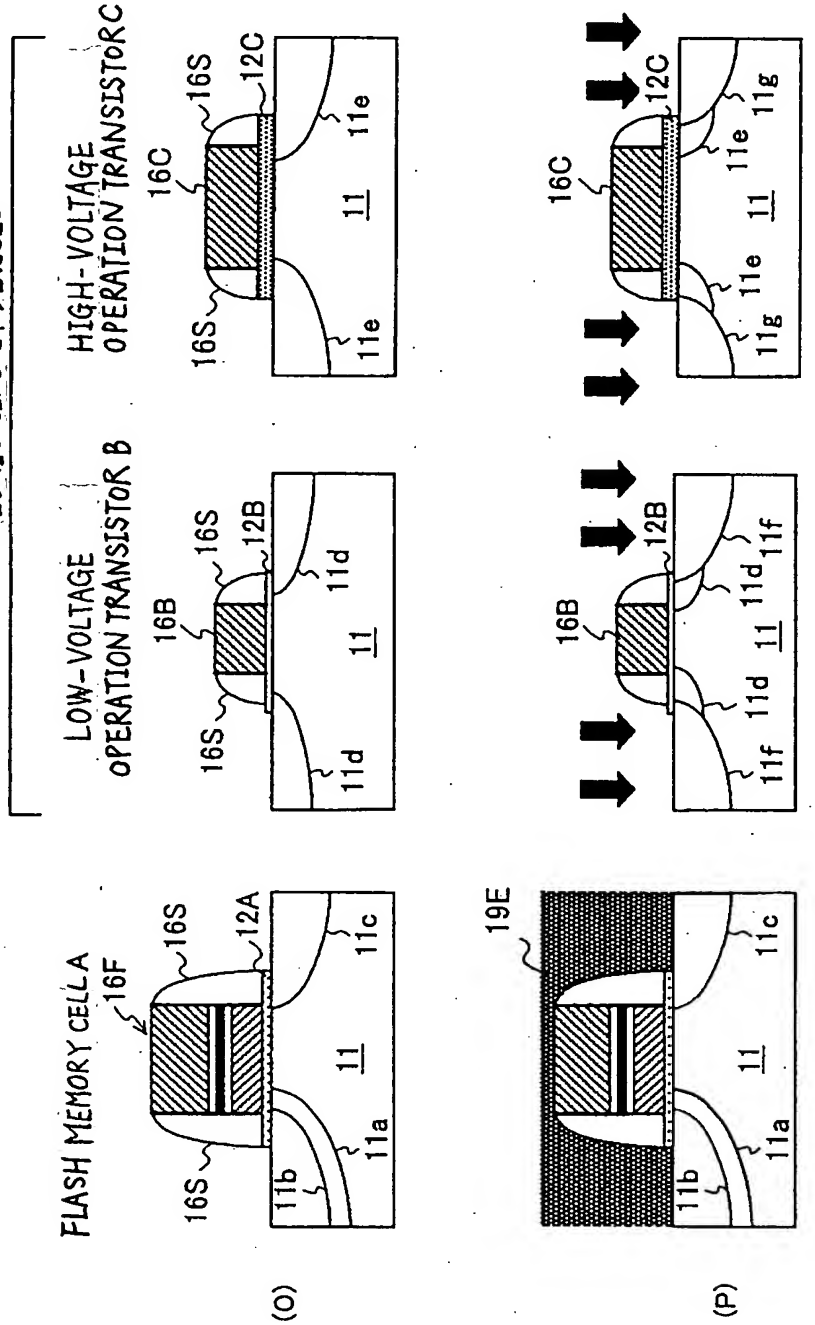
(FIG.7)

(M) AND (N) ARE DIAGRAMS (7) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



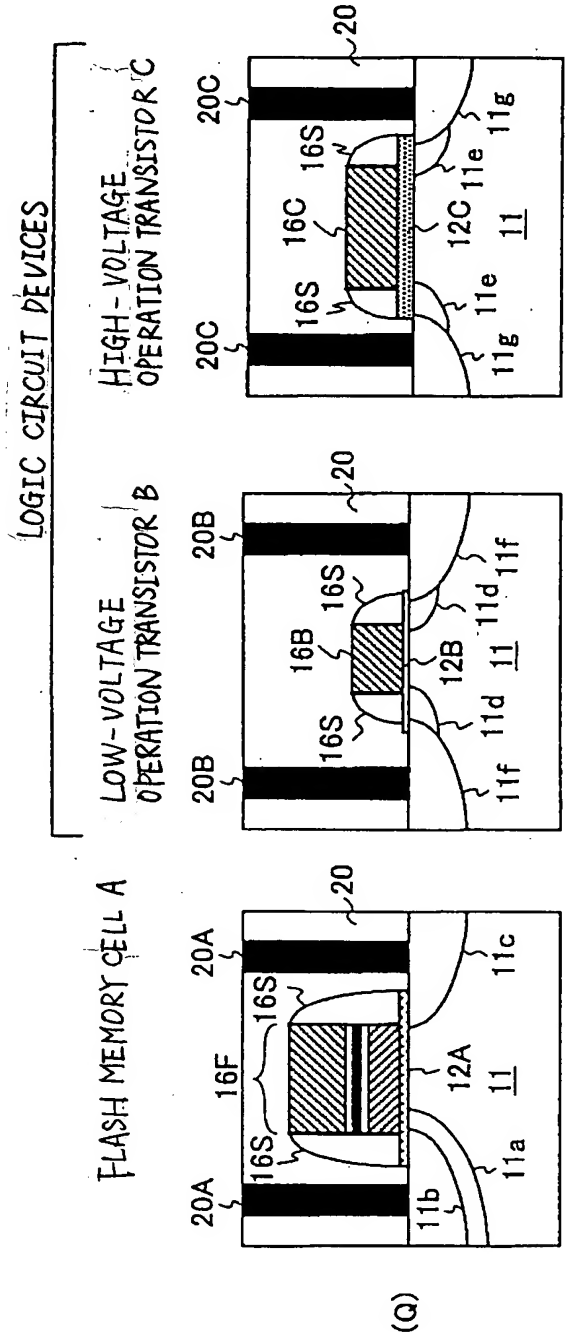
(FIG.8)

(O) AND (P) ARE DIAGRAMS (8) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATER CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



〔FIG.9〕

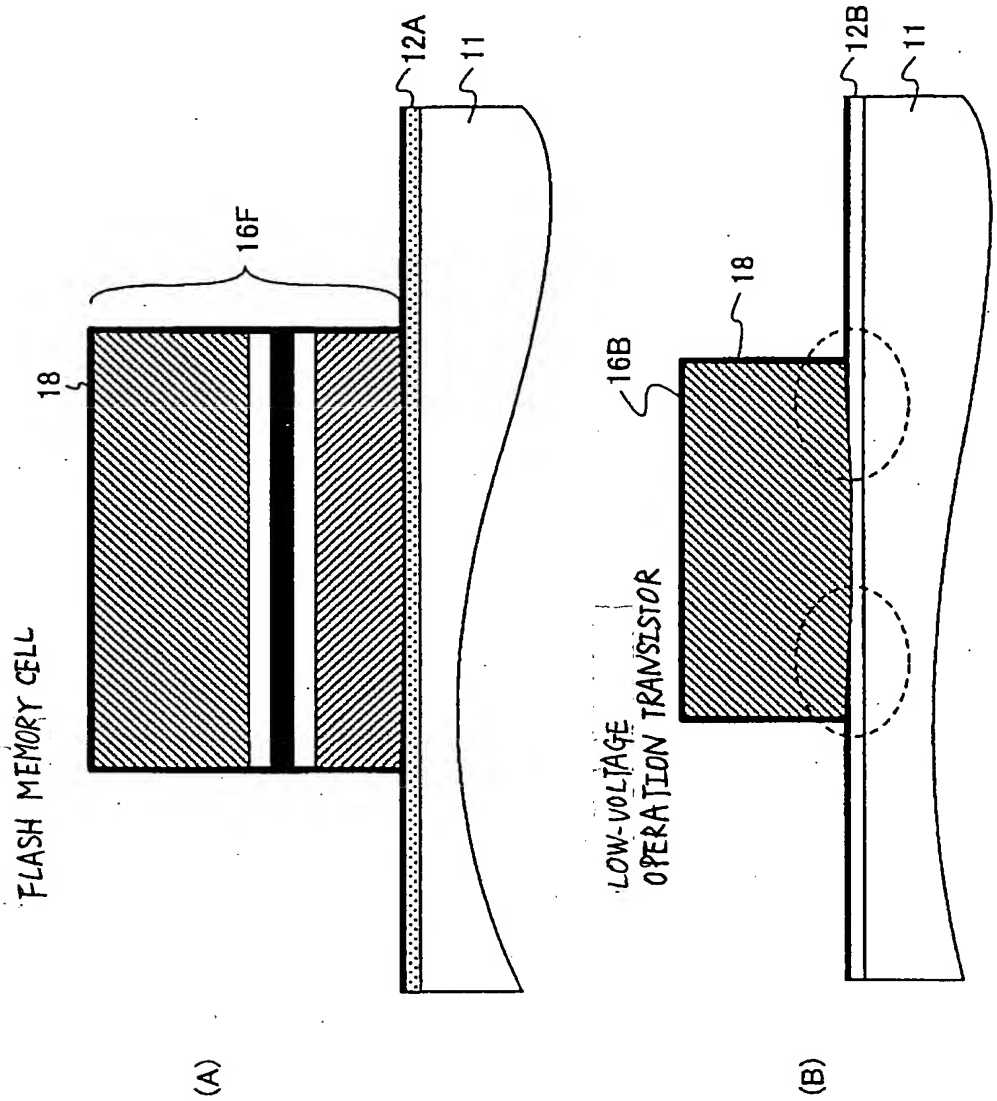
(Q) IS A DIAGRAM (8) SHOWING A PRODUCTION PROCESS OF A CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A FLASH MEMORY DEVICE OF A MULTILAYER GATE STRUCTURE.



(Q)

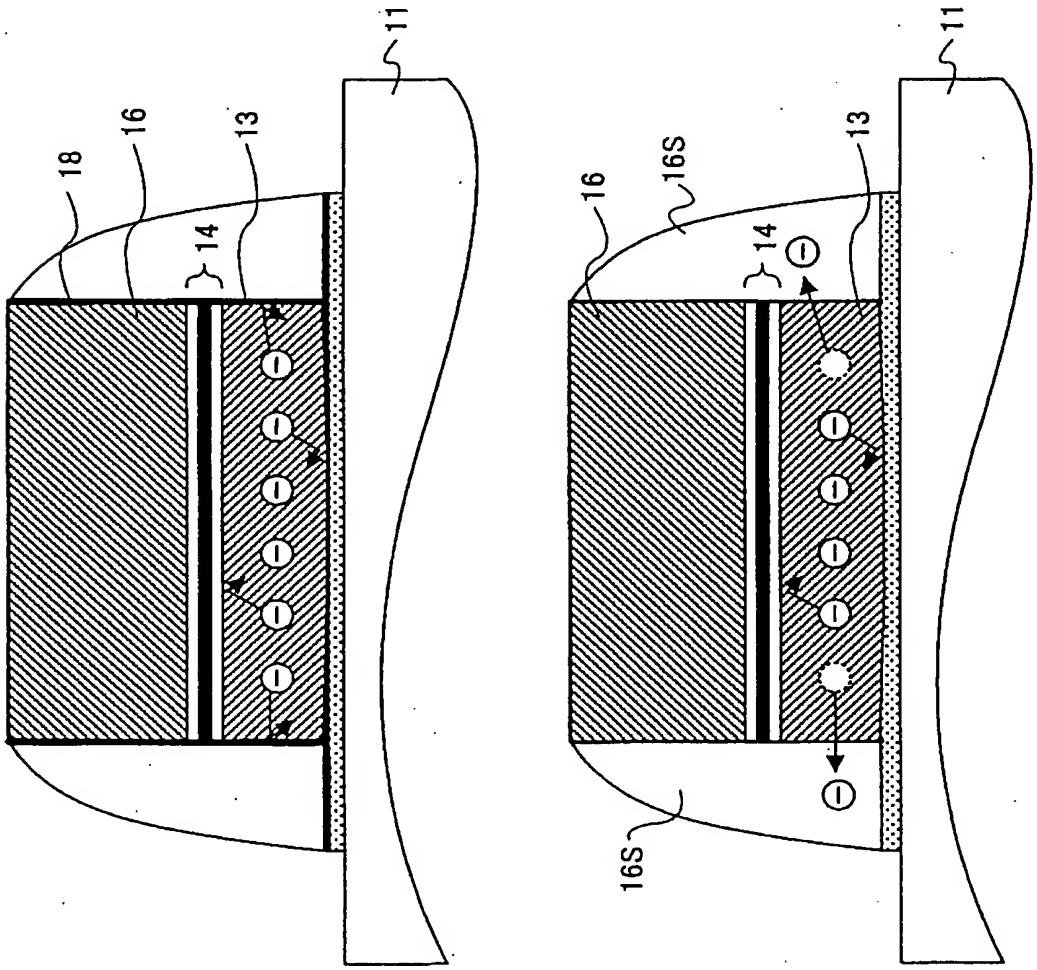
[FIG. 10]

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING A DISADVANTAGE OF THE CONVENTIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF THE MULTILAYER GATE STRUCTURE.



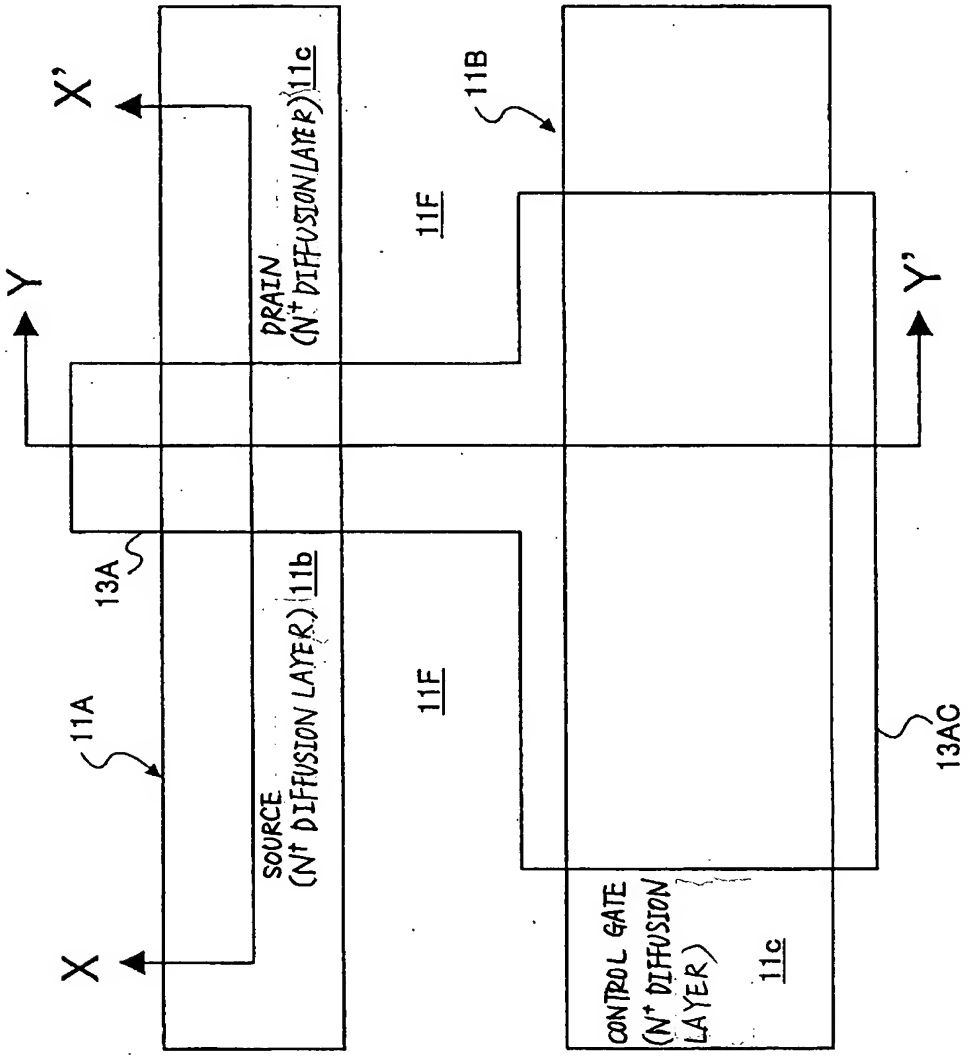
(FIG. 11)

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING A ROLE OF A PROTECTION OXIDE FILM EMPLOYED IN THE CONVENTIONAL MEMORY DEVICE OF THE MULTILAYER GATE STRUCTURE.



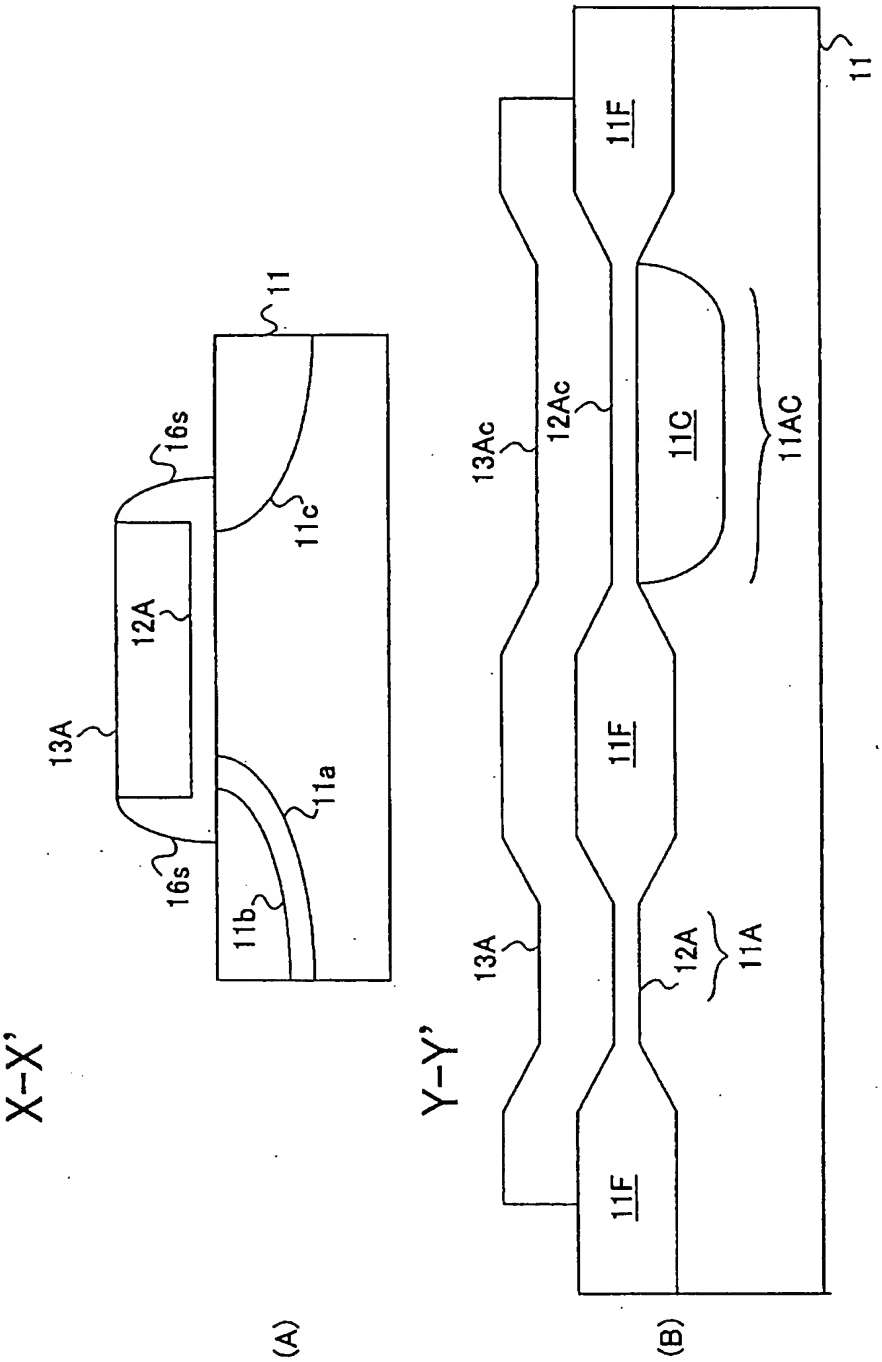
(FIG. 12)

PLAN VIEW OF A FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE ACCORDING TO RELATED ART OF THE PRESENT INVENTION.



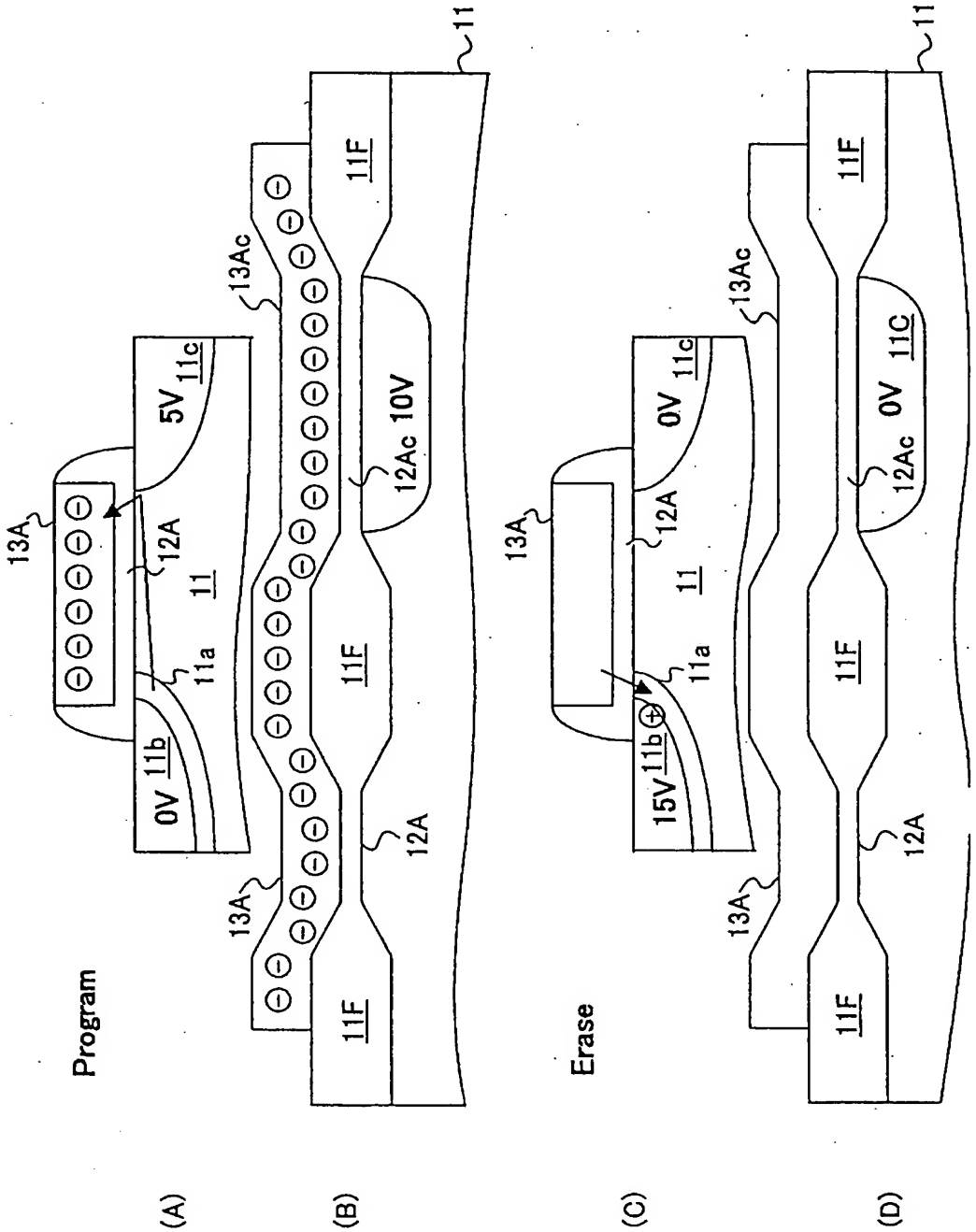
(FIG. 13)

(A) AND (B) ARE SECTIONAL VIEWS OF THE FLASH MEMORY DEVICE OF FIG. 12.



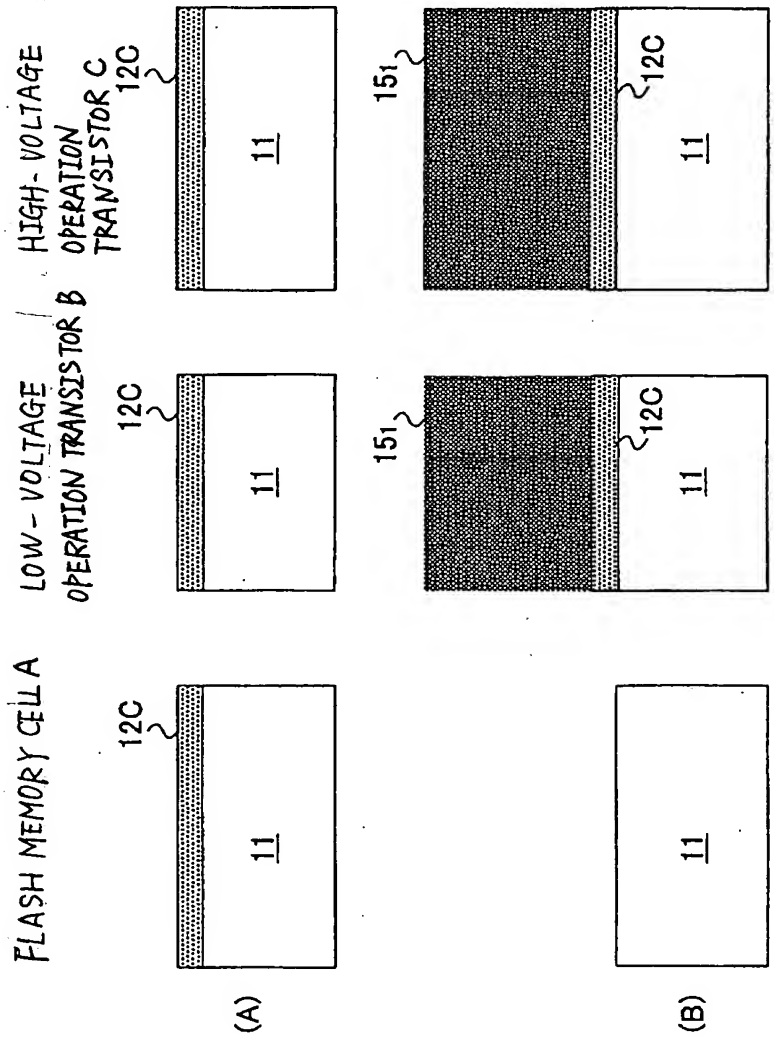
(FIG. 14)

(A) THROUGH (D) ARE DIAGRAMS FOR ILLUSTRATING WRITE AND ERASE OPERATIONS OF THE FLASH MEMORY DEVICE OF FIG. 12.



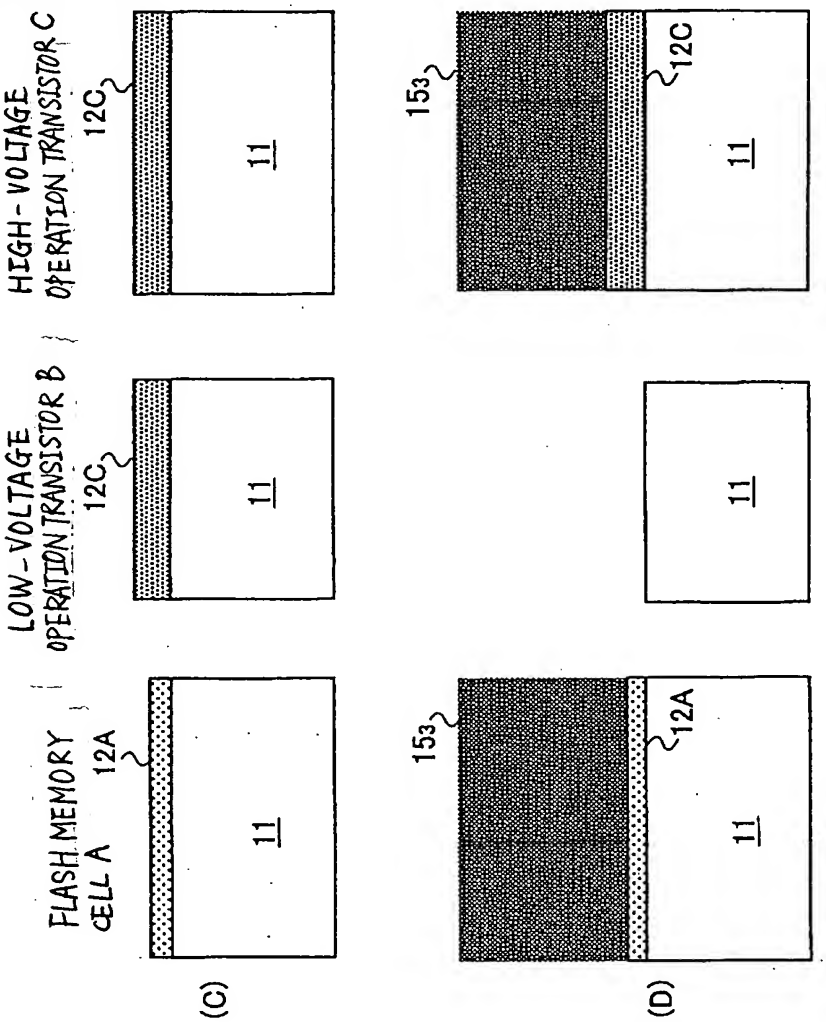
(FIG. 15)

(A) AND (B) ARE DIAGRAMS (I) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



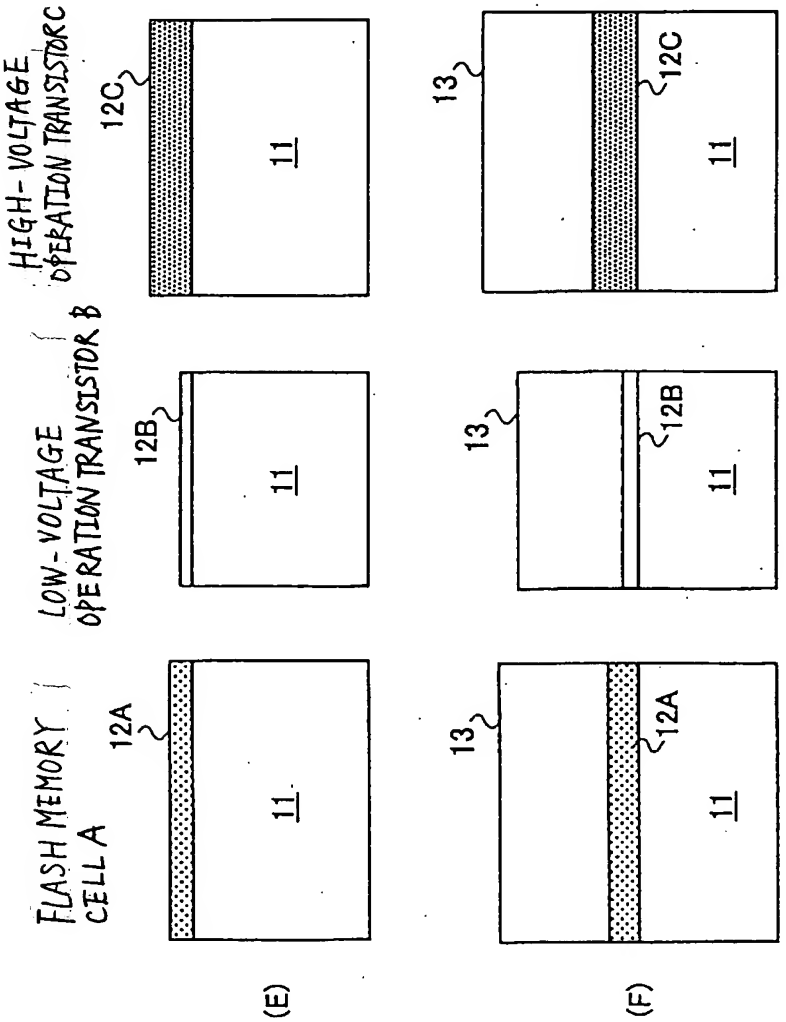
(FIG. 16)

(C) AND (D) ARE DIAGRAMS (2) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



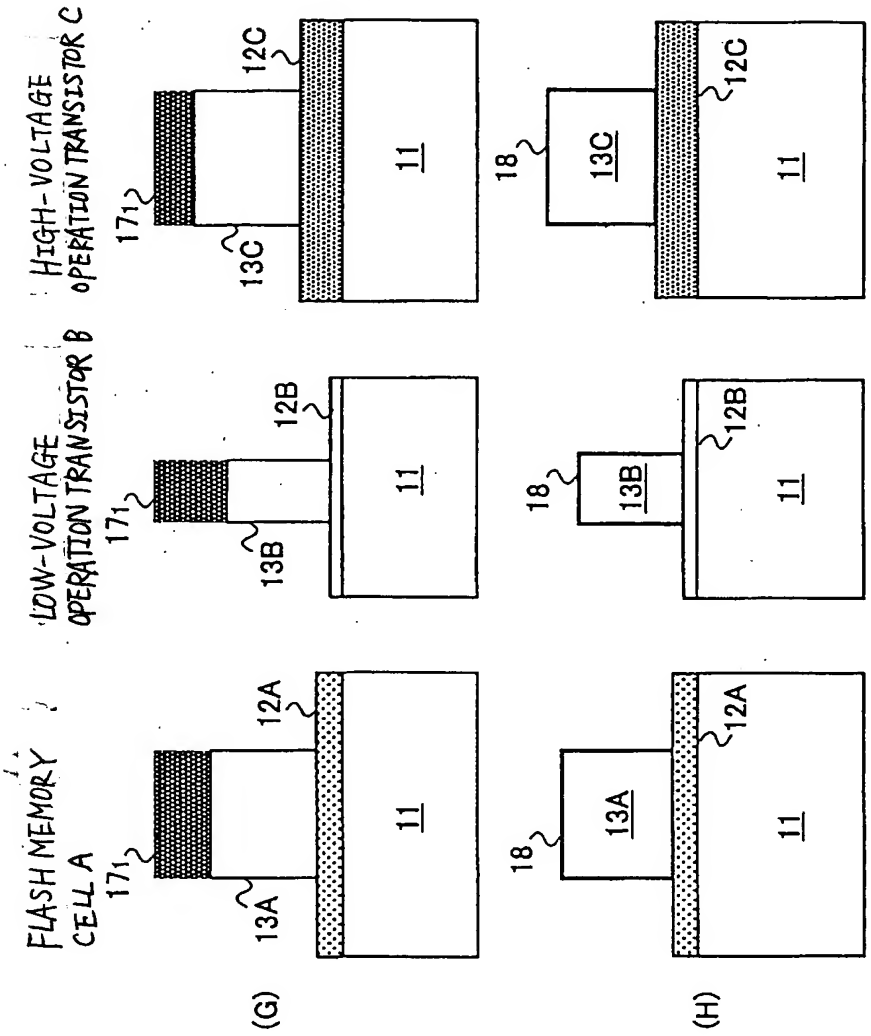
〔FIG.17〕

(E) AND (F) ARE DIAGRAMS (4) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



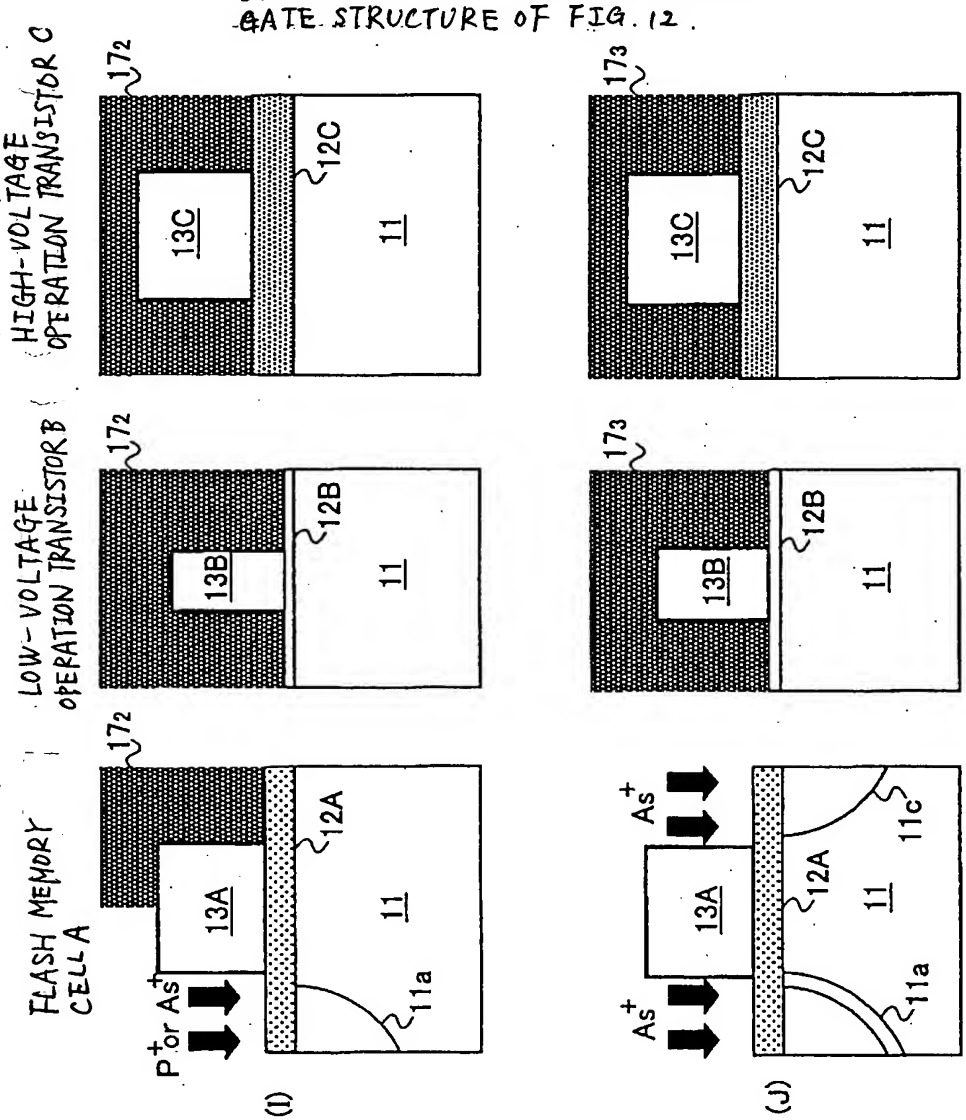
[FIG.18]

(G) AND (H) ARE DIAGRAMS (5) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



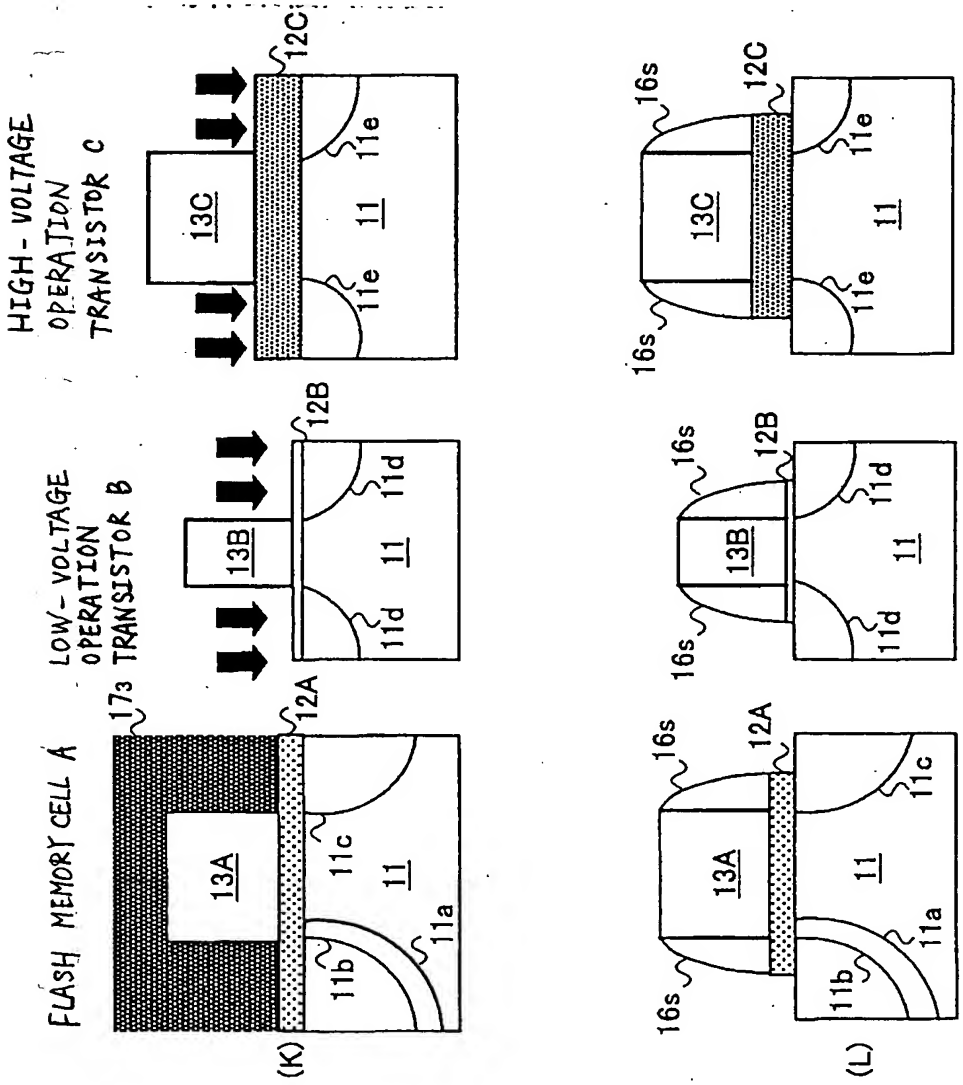
[FIG.19]

(I) AND (J) ARE DIAGRAMS (6) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



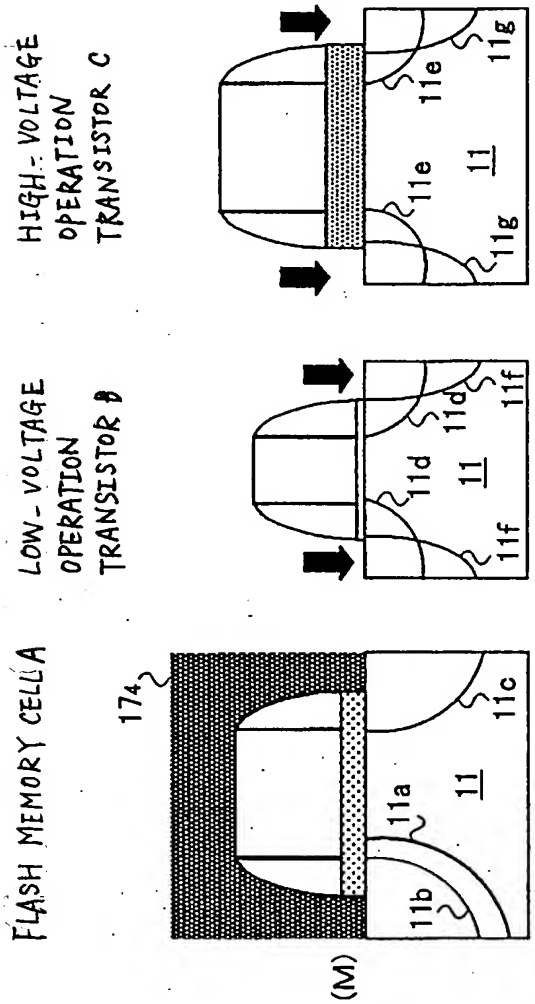
(FIG.20)

(K) AND (L) ARE DIAGRAMS (7) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



(FIG.21)

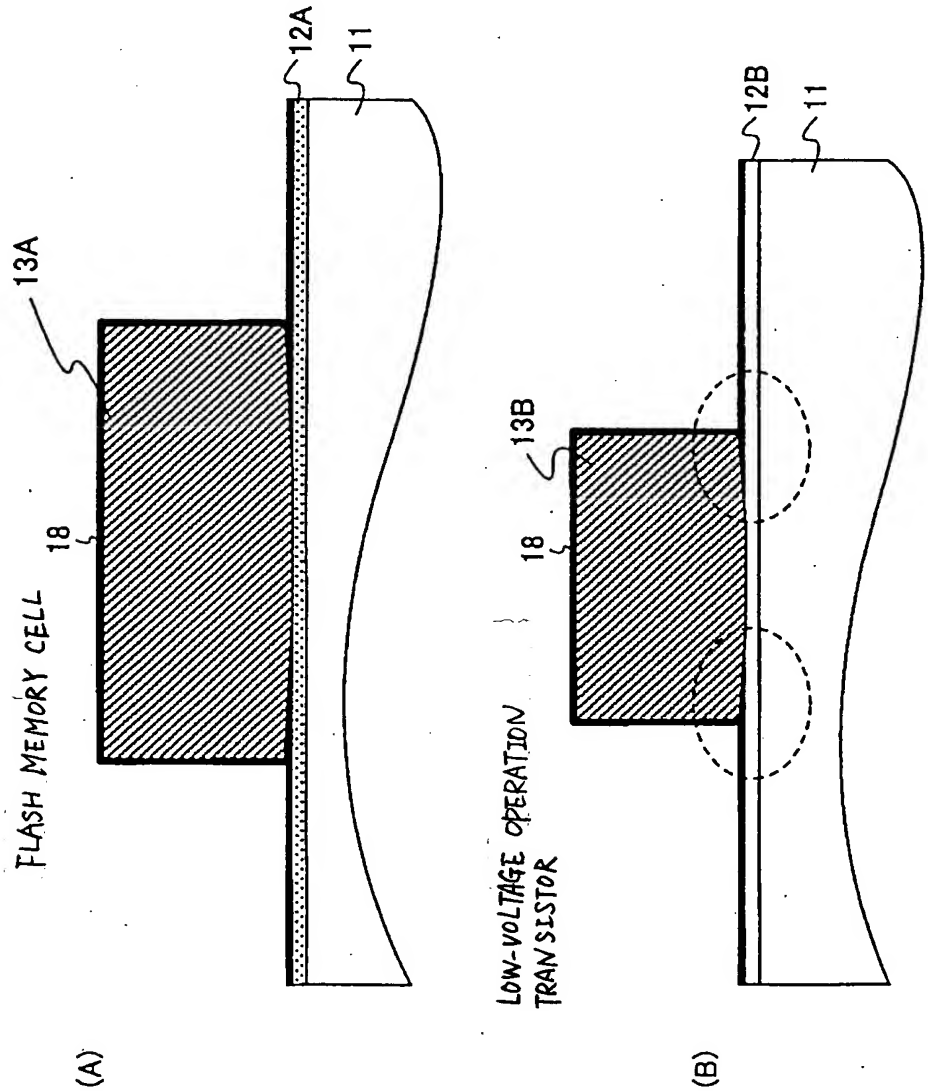
(M) IS A DIAGRAM (8) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG. 12.



(M)

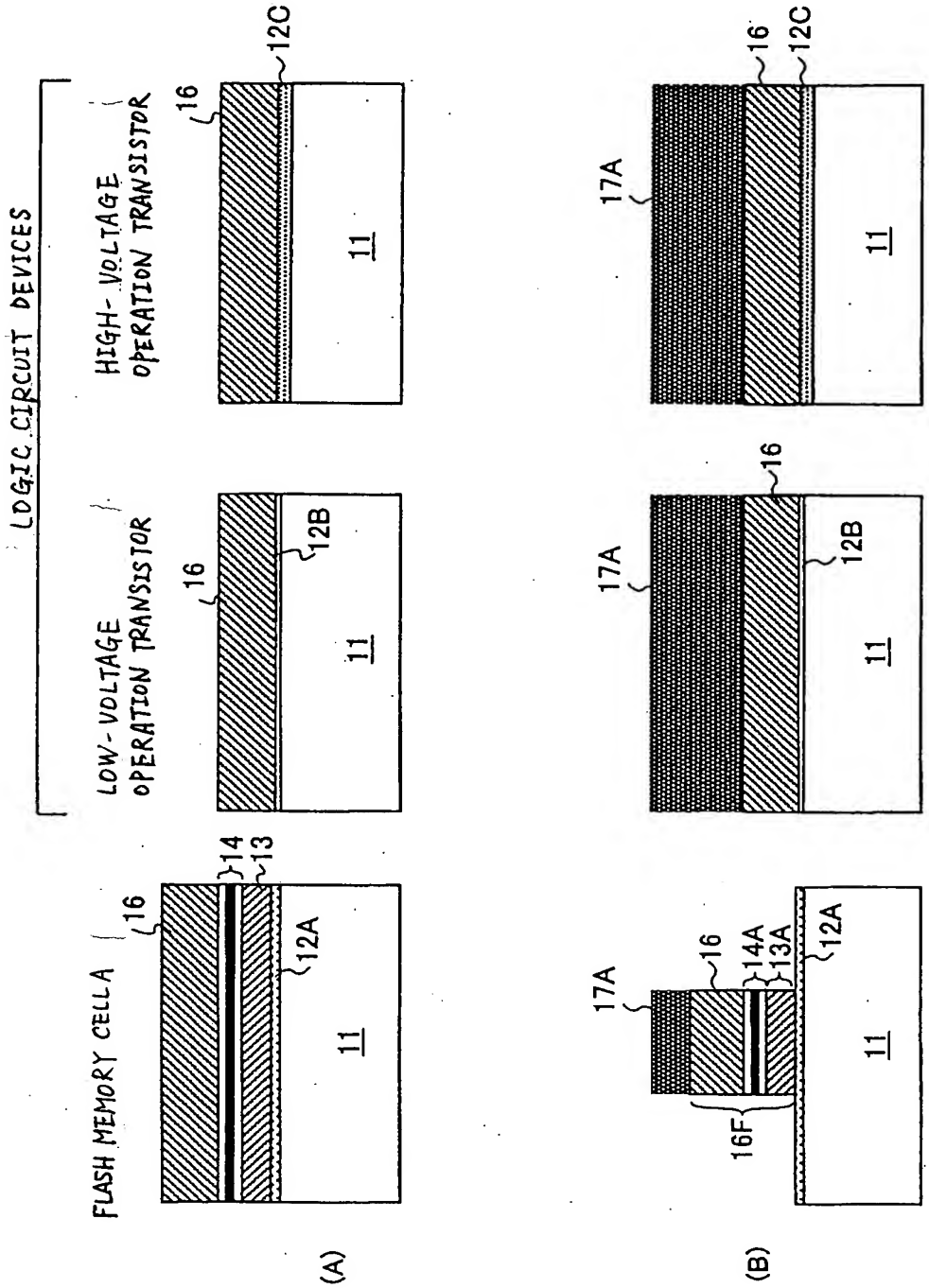
(FIG.22).

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING A DISADVANTAGE OF THE SEMICONDUCTOR INTEGATED CIRCUIT DEVICE INCLUDING THE FLASH MEMORY DEVICE OF A SINGLE-LAYER GATE STRUCTURE OF FIG.12.



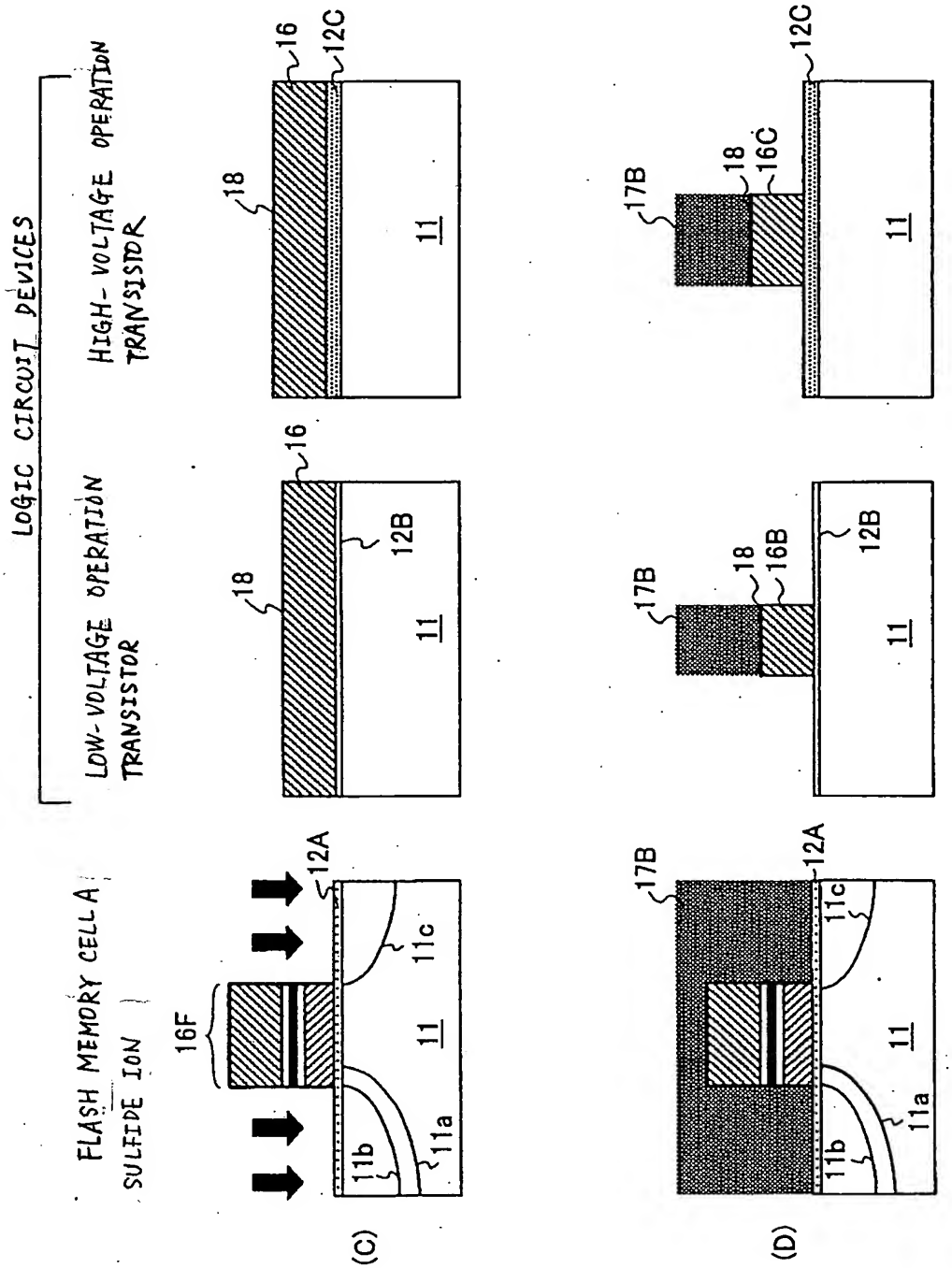
[FIG 23]

(A) AND (B) ARE DIAGRAMS(I) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A FIRST EMBODIMENT OF THE PRESENT INVENTION.



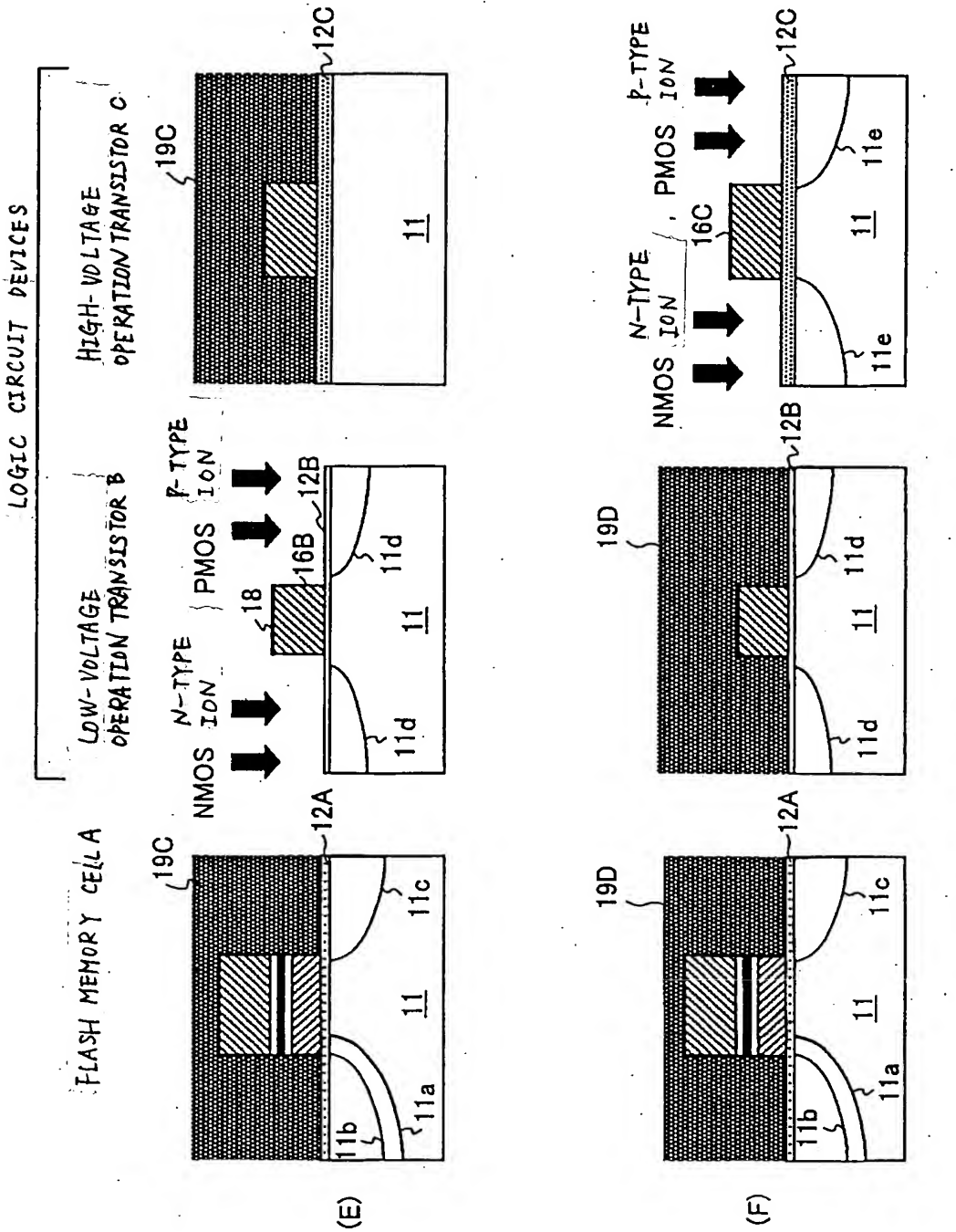
[FIG. 24]

(C) AND (D) ARE DIAGRAMS (2) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A FIRST EMBODIMENT OF THE PRESENT INVENTION.



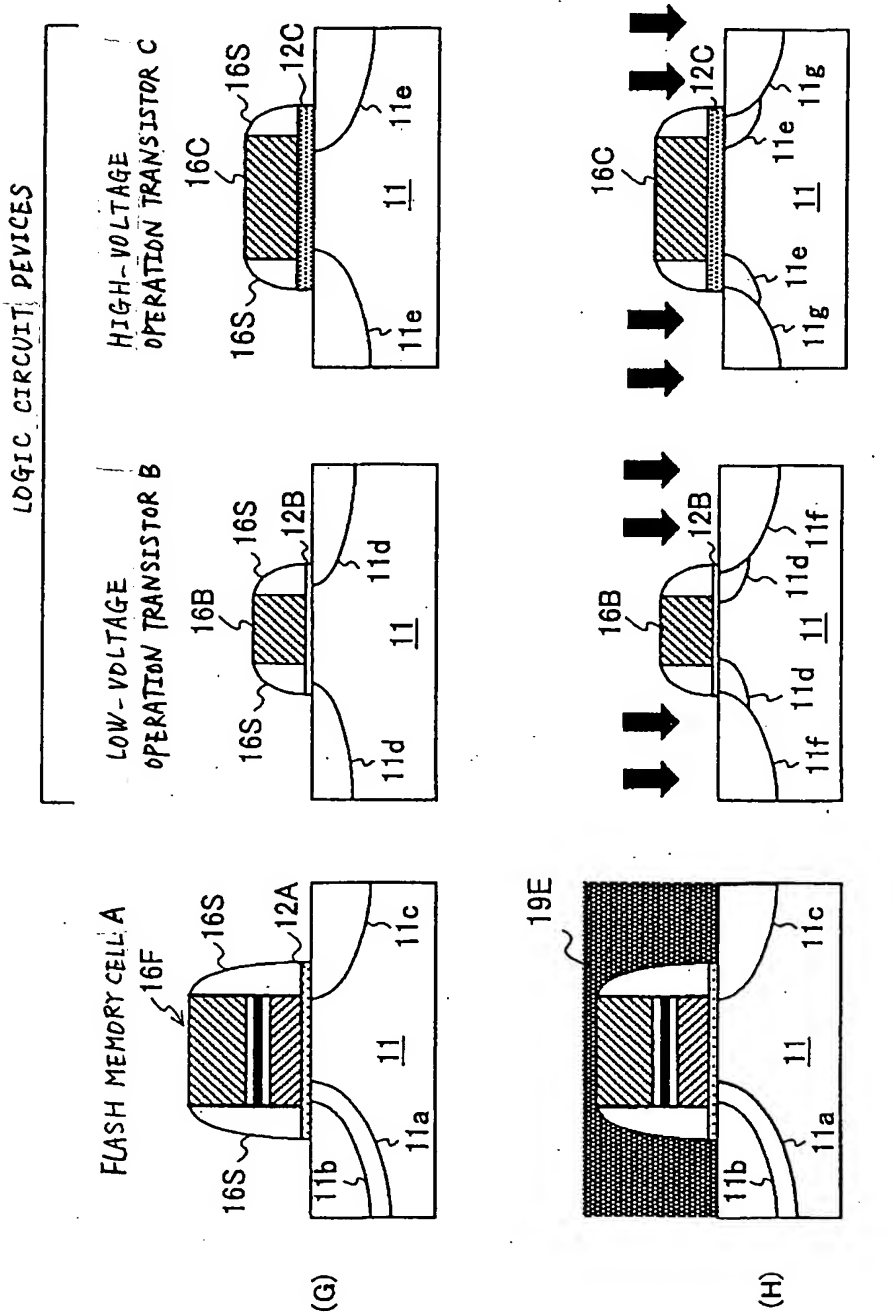
[FIG.25]

(E) AND (F) ARE DIAGRAMS (3) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A FIRST EMBODIMENT OF THE PRESENT INVENTION.



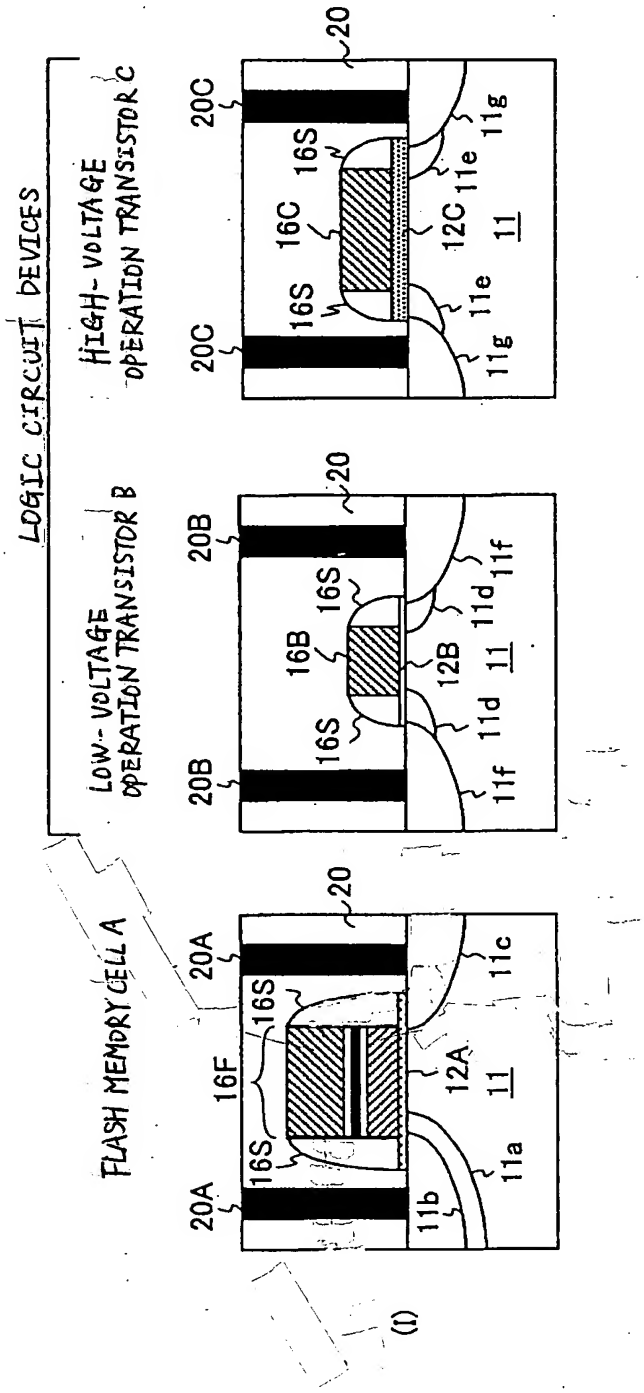
〔FIG 26〕

(G) AND (H) ARE DIAGRAMS (4) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A FIRST EMBODIMENT OF THE PRESENT INVENTION.



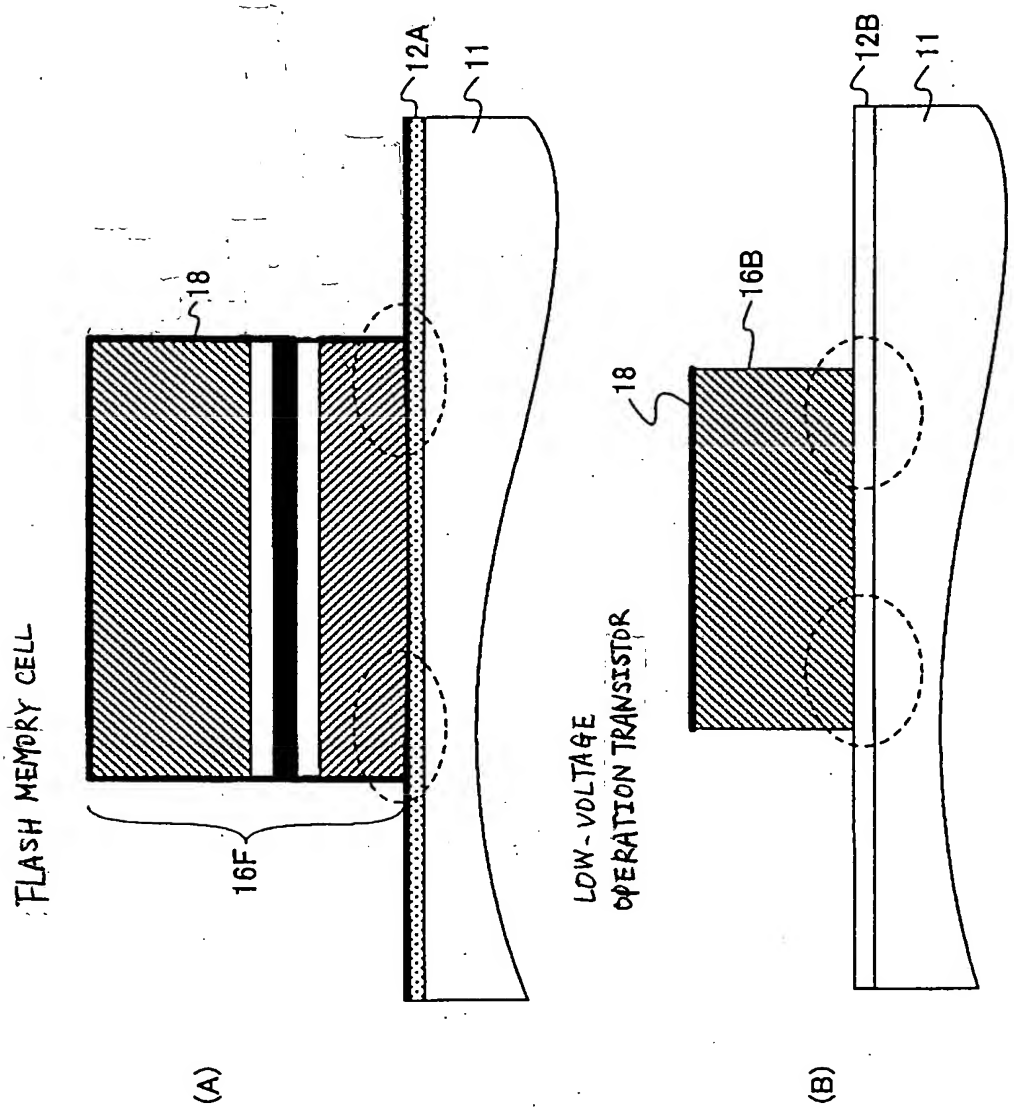
〔FIG.27〕

(I) IS A DIAGRAM (5) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A FIRST EMBODIMENT OF THE PRESENT INVENTION.



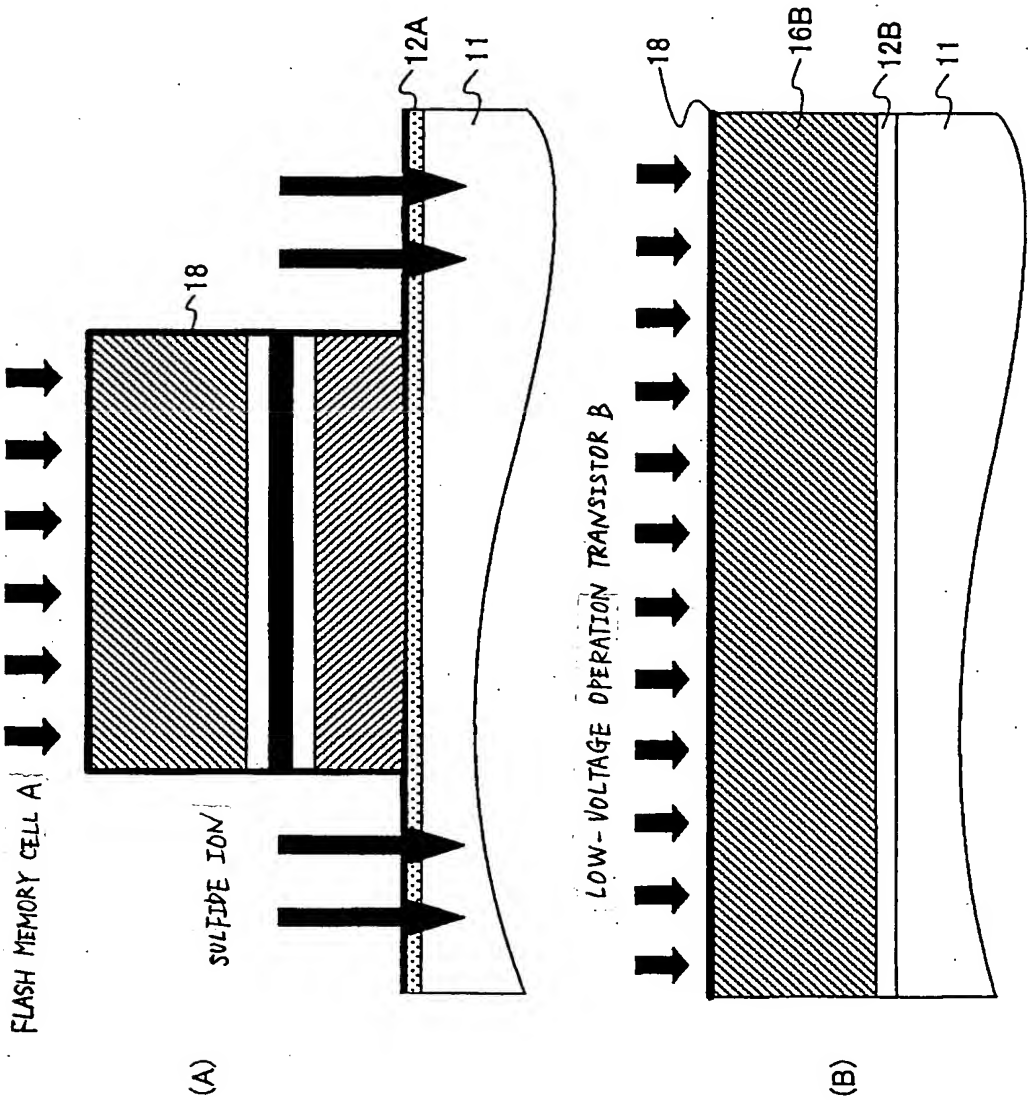
[FIG. 28]

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING AN EFFECT OF THE FIRST EMBODIMENT.



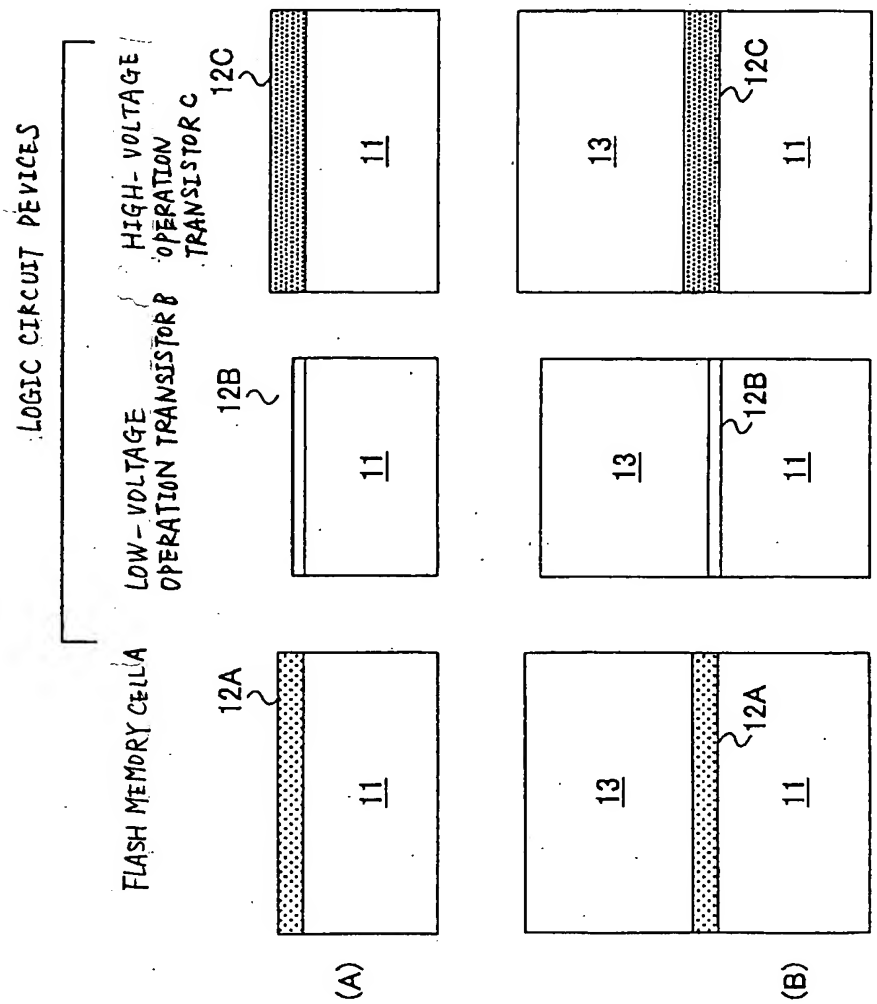
〔FIG.29〕

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING ANOTHER EFFECT OF THE FIRST EMBODIMENT.



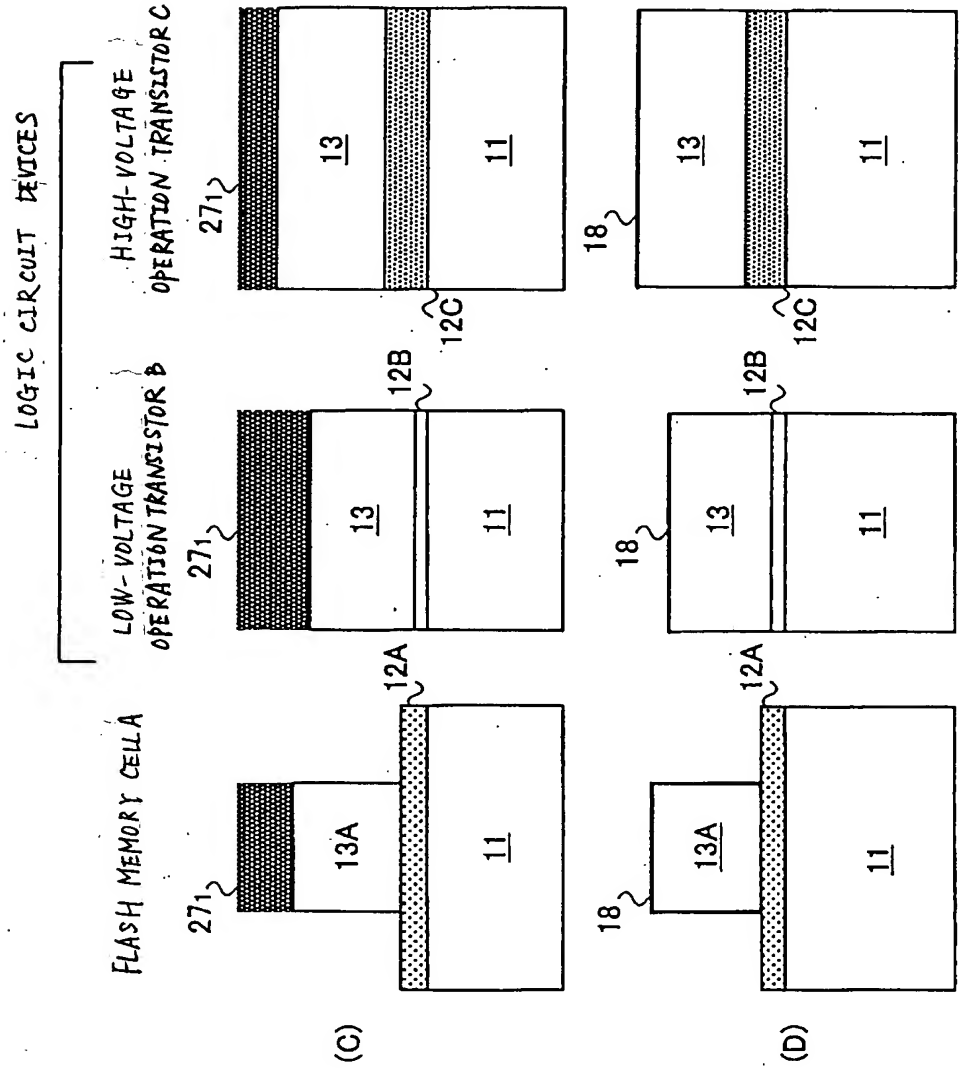
〔FIG 30〕

(A) AND (B) ARE DIAGRAMS (I) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A SECOND EMBODIMENT OF THE PRESENT INVENTION.



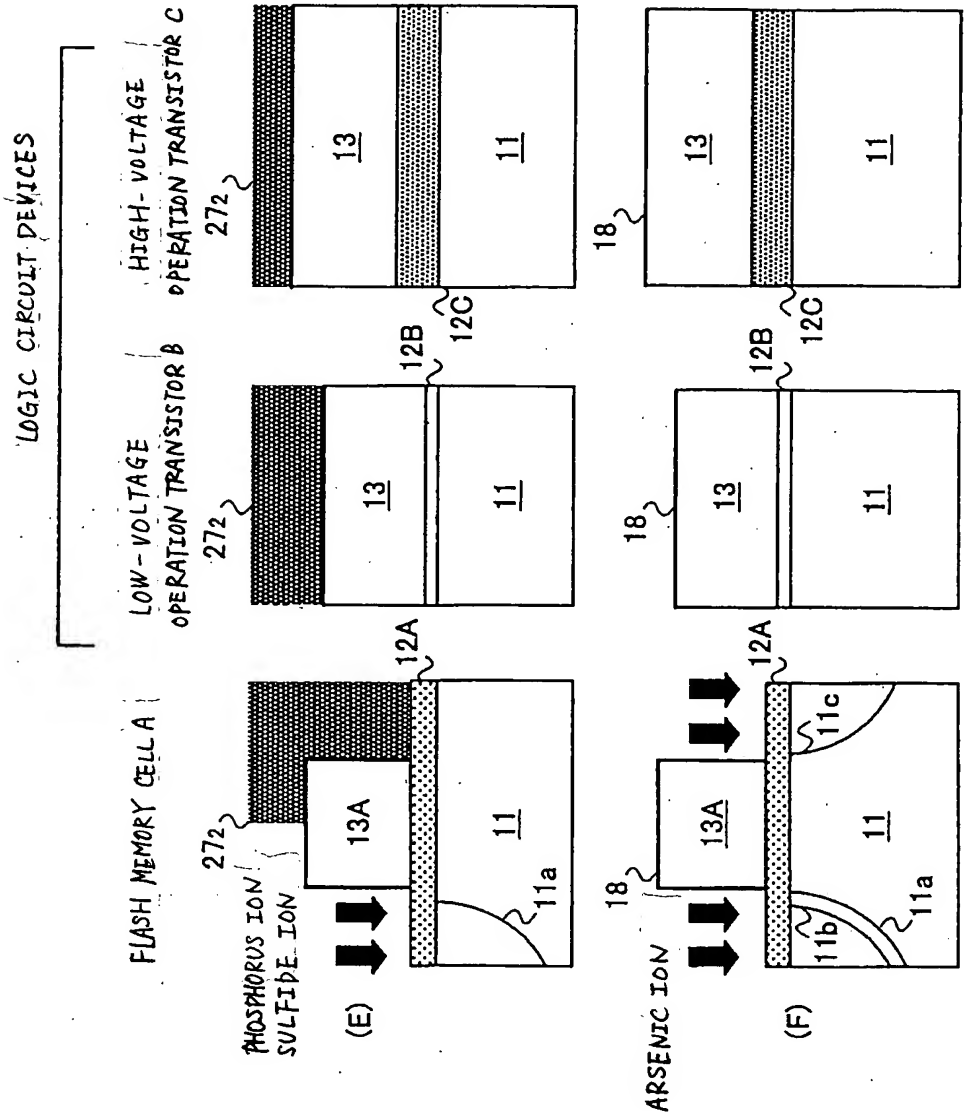
〔FIG. 31〕

(C) AND (D) ARE DIAGRAMS (2) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A SECOND EMBODIMENT OF THE PRESENT INVENTION.



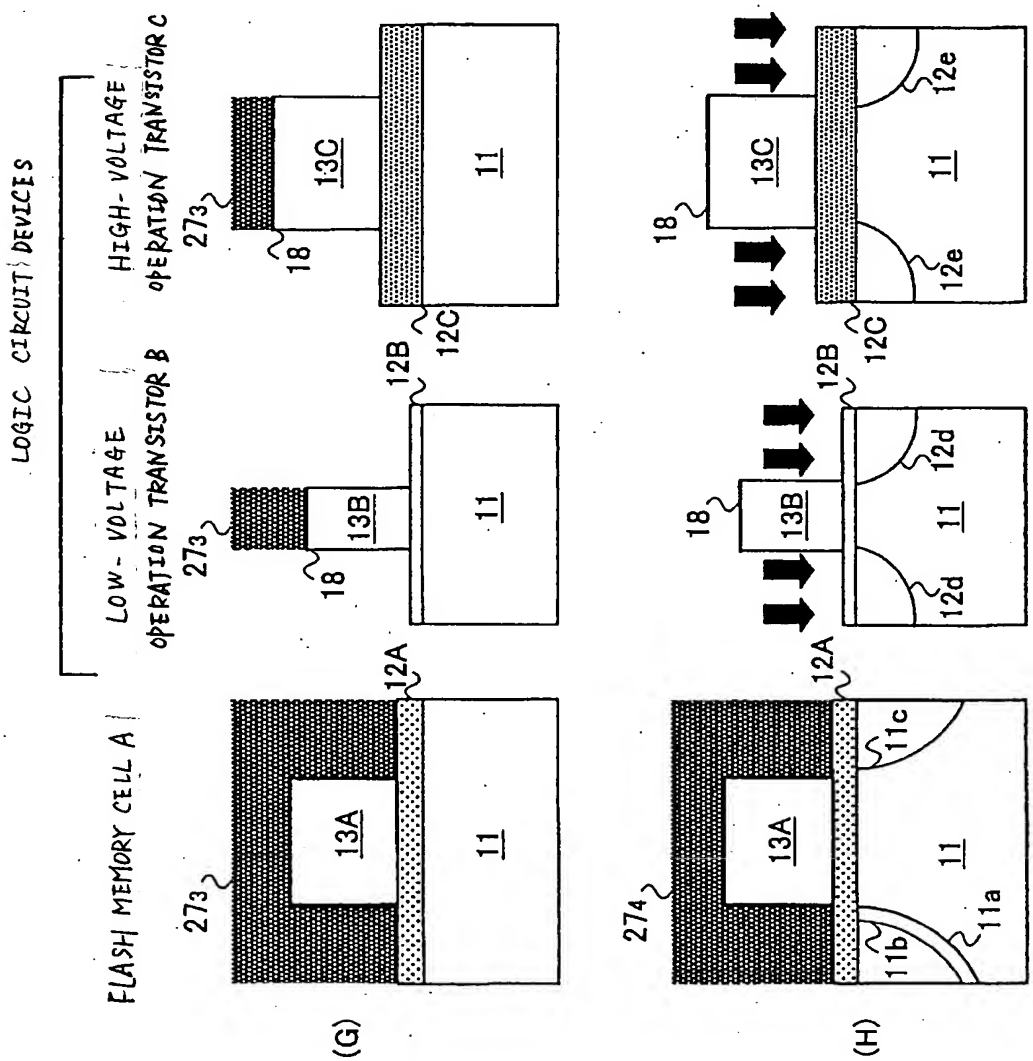
(FIG. 32)

(E) AND (F) ARE DIAGRAMS (3) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A SECOND EMBODIMENT OF THE PRESENT INVENTION.



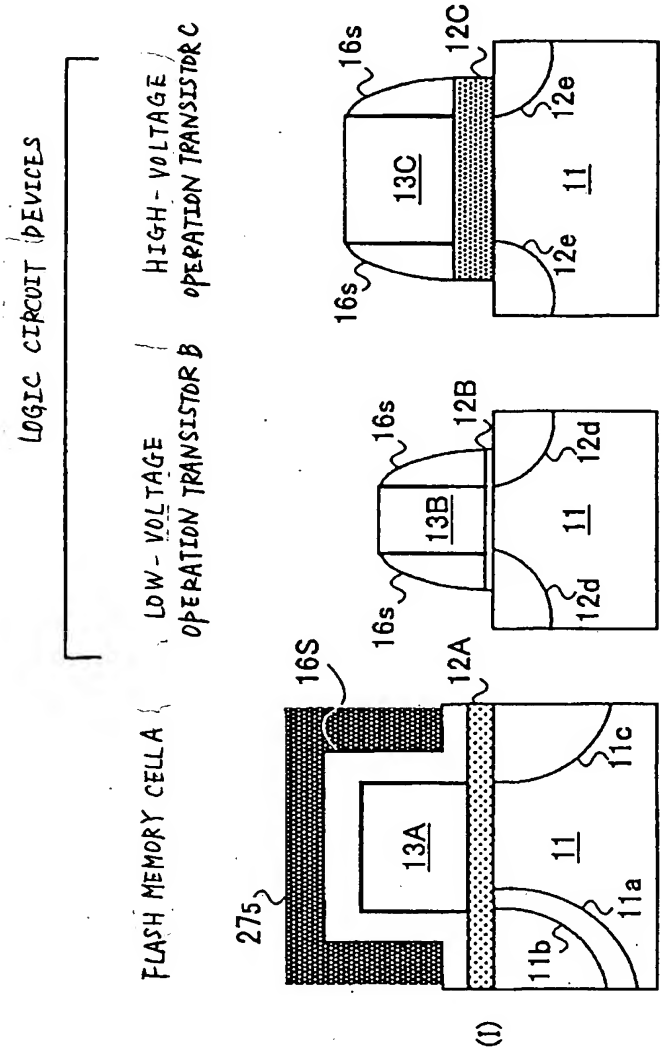
[FIG. 33]

(G) AND (H) ARE DIAGRAMS (4) SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A SECOND EMBODIMENT OF THE PRESENT INVENTION.



〔FIG.34〕

(I) IS A DIAGRAM SHOWING A PRODUCTION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE ACCORDING TO A SECOND EMBODIMENT OF THE PRESENT INVENTION.



〔FIG.35〕

(A) AND (B) ARE DIAGRAMS FOR ILLUSTRATING EFFECTS OF THE SECOND EMBODIMENT